Access DB# 99930

SEARCH REQUEST FORM

152

Scientific and Technical Information Center

Requester's Full Name: Peng Ke Examiner #: 79571 Date: 7/28/03
Art Unit: 2174 Phone Number 30 5715 Serial Number: 09742523
Mail Box and Bldg/Room Location: 4C30 Results Format Preferred (circle): PAPER DISK E-MAIL

If more than one search is submitted, please prioritize searches in order of need.

****

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: System and method for accessing resources of a hardware device in a [illegible] program

Inventors (please provide full names): [illegible]

Earliest Priority Filing Date: 12/20/00

For Sequence Searches Only *Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.*

A GUI system that displays the list of register modes of a hardware, and allows the user to configure these modes

07-29-03 A08:44 IN

****

STAFF USE ONLY	Type of Search	Vendors and cost where applicable
Searcher: Conference Logan	NA Sequence (#)	STN
Searcher Phone #: 305-7200	AA Sequence (#)	Dialog ✓
Searcher Location: CP3-3C	Structure (#)	Questel/Orbit
Date Searcher Picked Up: 7/30/3	Bibliographic	Dr.Link
Date Completed: 7/30/3	Litigation	Lexis/Nexis
Searcher Prep & Review Time: 6 Cmin	Fulltext ✓	Sequence Systems
Clerical Prep Time:	Patent Family	WWW/Internet
Online Time: 270 min	Other	Other (specify)

PTO-1590 (8-01)

STIC Search Report
EIC 2100

Scientific & Technical Information Center
USPTO

STIC Database Tracking Number: 99930

TO: Peng (Simon) Ke
Location: 4C30
Art Unit : 2174
Wednesday, July 30, 2003

Case Serial Number: 09/742523

From: Geoffrey St. Leger
Location: EIC 2100
PK2-4B30
Phone: 308-7800

geoffrey.stleger@uspto.gov

Search Notes

Dear Examiner Ke,

Attached please find the results of your search request for application 09/742523. I searched Dialog's foreign patent files, technical databases, product announcement files and general files.

Please let me know if you have any questions.

Regards,

Geoffrey St. Leger
4B30/308-7800

sira
Search and Information Resources Administration

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File   8:Ei Compendex(R) 1970-2003/Jul W3
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File 438:Library Lit. & Info. Science 1984-2003/Jun
         (c) 2003 The HW Wilson Co
File 248:PIRA 1975-2003/Jul W4
         (c) 2003 Pira International

Set     Items   Description
S1      18958   AU=(KING, J? OR KING J? OR ROGERS S? OR ROGERS, S?)
S2         21   S1 AND REGISTER? ?
S3         18   RD (unique items)
S4         17   S3 NOT PY=2001:2003
```

4/5/3 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

03669181 INSPEC Abstract Number: C90048941
Title: Using interactive computer graphics to simulate the dynamic internal processes of a simple computer
Author(s): **King, J.**
Author Affiliation: Dept. of Electr. Eng., Univ. of the Pacific, Stockton, CA, USA
Conference Title: Simulation in Engineering Education Including Supplemental Papers. Proceedings of the SCS Multiconference on Modeling and Simulation on Microcomputers p.46-50
Editor(s): Ward, M.
Publisher: SCS, San Diego, CA, USA
Publication Date: 1990 Country of Publication: USA 102 pp.
ISBN: 0 911801 65 0
Conference Date: 17-19 Jan. 1990 Conference Location: San Diego, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); Practical (P)
Abstract: In an era when educators are increasingly using computers to assist in the educational process, it seems appropriate that computer engineering teachers should be doing so as well. As computer professionals attempt to explain design principles, they tend to draw **registers** and the like on a blackboard and then tell the students how bits move though a maze of circuitry. unfortunately, many students simply do not get the point. 'SIM 4*4' is a PC-based computer simulation program that was born of the desire to use something better than a black-board to illustrate the operation of a computer. Written in C, it simulates a 16-instruction computer that has 4-bit address and data buses (hence the '4*4' 'SIM4*4'). The video display of 'SIM4*4' portrays all the necessary **registers** of a minimal computer, plus the CONTROL, MEMORY, ALU and I/O sections. During a simulation session students enter assembly code programs, observe their conversion to binary, and then interact with the computer as it simulates execution of the programs one clock cycle at a time. (3 Refs)
Subfile: C
Descriptors: computer graphics; computer science education; digital simulation; educational computing; interactive systems; software packages
Identifiers: digital simulation; interactive computer graphics; dynamic internal processes; simple computer; SIM 4*4; PC-based computer simulation program; C; assembly code programs
Class Codes: C7810C (Computer-aided instruction); C0220 (Education and training); C6130B (Graphics techniques)

4/5/5 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

01272852 INSPEC Abstract Number: C78031267
Title: Controlling program instructions in a digital computer
Author(s): Blake, D.R.; **King, J.G.**
Author Affiliation: IBM, Armonk, NY, USA
Journal: IBM Technical Disclosure Bulletin vol.20, no.9 p.3419-20
Publication Date: Feb. 1978 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: The method is based on a count in modulo M by an increment N, where N may be a variable. The process is designed so that the execution of the instruction is performed in a general **register** computer having two **registers** R1 and R2, each divided into two segments defined as R1-HI, R1-LO, R2-HI, R2-LO. In the execution of an instruction R1-HI contains the modulus, R1-LO contains the count, R2-LO contains the increment, R2-HI does not participate. (0 Refs)
Subfile: C
Descriptors: supervisory and executive programs

Identifiers: count, modulo M; increment N; general **register** computer; program execution control
Class Codes: C6150J (Operating systems)

4/5/13 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1649350 NTIS Accession Number: AD-A248 707/2
Future of Logistics Automation
(Study project)
Lauer, D. M. ; **King, J. C.**
Army War Coll., Carlisle Barracks, PA.
Corp. Source Codes: 025057000; 403565
15 Mar 92 47p
Languages: English
Journal Announcement: GRAI9215
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NTIS Prices: PC A03/MF A01
Country of Publication: United States
Since the mid-1960s the Army has integrated automation into almost every aspect of logistics. The Army Logistician's start point for fielding an automated system was little more than a sophisticated accounting machine, the National Cash **Register** model NCR 500. The NCR 500 did nothing more than automate an existing manual process. In the next thirty years the Army's logistics community has done little more than continue to automate manual processes. Each branch, and branch subset, has independently developed their system, because they felt their functions to be unique. Today we have logistics systems that do not share information with other logistics systems and that have different names for the same thing. Logisticians have a difficult time understanding their own automated systems. The rest of the Army generally does not try. The Army tactical commander does not have direct, easy, access to logistics information regarding his unit's logistical status. Most battalion and brigade commanders, logisticians and non-logisticians alike, feel that logistics systems are developed without a view towards Army needs. This paper will look at where Army logistics automation has been, where it is today, and where current planning will take it in the future. The paper concludes with where the author thinks logistics automation should be going, why and how. This paper is not a technical treatise on logistics automation. There will be no discussions of what goes in card column 39 nor what AOA card does within the system. It is rather a concerned conceptual look at the topic, with a view towards Army logistics for the remainder of this century and into the twenty-first century.

File 347:JAPIO Oct [redacted]6-2003/Mar(Updated 030703)
(c) 2003 JPO & JAPIO
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200348
(c) 2003 Thomson Derwent

Set	Items	Description
S1	228318	REGISTER? ?
S2	28421	S1(5N)(ACCESS??? OR READ??? OR SCAN???? OR RETRIEV??? OR OBTAIN??? OR GET???? OR POLL??? OR CHECK??? OR EXAMIN? OR ANALYZ??? OR ANALYS? OR INSPECT??? OR SCRUTINI? OR LOOK??? OR OBSERV? OR MONITOR? OR ACQUIR??? OR ACQUISITION OR TAP????)
S3	36356	S1(5N)(INPUT??? OR WRIT??? OR MANIPULAT? OR CONFIGUR?)
S4	25289	(GRAPHIC? OR WINDOW?)(2W)INTERFACE? ? OR GUI OR GUIS OR BROWSER? ? OR GRAPHIC??(2W)(SCREEN? ? OR DISPLAY? ? OR PANE?? OR MONITOR? ? OR PROGRAM? OR APPLICATION? ? OR SOFTWARE)
S5	1311988	CAD OR CAM OR CAE OR COMPUTER()(ASSISTED OR AIDED)()(DRAWING OR DESIGN? OR MANUFACTUR??? OR ENGINEERING) OR DESIGN??? OR DIAGRAM? OR SIMULAT? OR EMULAT???
S6	10855	DEVICE? ?(5N)DRIVER? ?
S7	6903	S2:S3 AND S4:S5
S8	19	S7 AND S6
S9	275	S7 AND IC=G09G
S10	4214	S7 AND IC=G06F
S11	162649	CAD OR CAM OR CAE OR COMPUTER()(ASSISTED OR AIDED)()(DRAWING OR DESIGN? OR MANUFACTUR??? OR ENGINEERING)
S12	404	S2:S3 AND (S4 OR S11)
S13	105	S12 AND IC=G09G
S14	32072	S1(5N)(ACCESS??? OR READ??? OR SCAN???? OR RETRIEV??? OR OBTAIN??? OR GET???? OR POLL??? OR CHECK??? OR EXAMIN? OR ACQUIR??? OR ACQUISITION OR TAP???? OR WRIT??? OR MANIPULAT? OR CONFIGUR? OR FETCH???)
S15	226	S14 AND (S4 OR S11)
S16	223	S15 NOT S8
S17	49	S16 AND IC=G09G
S18	174	S16 NOT S17
S19	116	S18 AND IC=G06F
S20	23	S14/TI AND S18
S21	77284	SIMULAT? OR EMULAT???
S22	399	S14 AND S21
S23	52	S14/TI AND S21
S24	49	S23 NOT(S8 OR S17 OR S20)

17/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06806764 **Image available**
GRAPHICS DISPLAY DEVICE

PUB. NO.: 2001-034248 [JP 2001034248 A]
PUBLISHED: February 09, 2001 (20010209)
INVENTOR(s): HIRATA KEN
KAIZE TETSUYA
APPLICANT(s): TOSHIBA CORP
TOSHIBA AVE CO LTD
APPL. NO.: 11-207539 [JP 99207539]
FILED: July 22, 1999 (19990722)
INTL CLASS: **G09G-005/00** ; **G09G-005/02**

ABSTRACT

PROBLEM TO BE SOLVED: To increase the redrawing speed of picture resetting when the power source of a monitor is turned off or a channel is changed by reducing the colors of a graphics image displayed right before redrawing, and storing the graphics image.

SOLUTION: When a power-OFF indication is inputted from a remote control photodetection part 102, the remote control photodetection part 102 informs a power source processing part 113 of it and further the power source processing part 112 informs a memory interface 108, a color reducing process part 111, and a display processing part 112. The color reducing process part 111 reads in the displayed graphics data from an external memory 105 once the power- OFF indication is inputted. The addresses of a **graphics display** area needed for the **read** are set in **registers** of the memory interface part 108. The read-out graphics data are processed by color reduction using a conversion table indicated by the CPU 115 and written to a free area of the external memory 105 through the memory interface part 108 again.

17/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05690989 **Image available**
ARITHMETIC METHOD AND **GRAPHICS DISPLAY** DEVICE

PUB. NO.: 09-305789 [JP 9305789 A]
PUBLISHED: November 28, 1997 (19971128)
INVENTOR(s): ABE KATSURA
NAKATSUKA YASUHIRO
IIMURA ICHIRO
SATO JUN
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-125569 [JP 96125569]
FILED: May 21, 1996 (19960521)
INTL CLASS: [6] G06T-015/00; G06F-007/02; G06T-011/00; **G09G-005/36** ; **G09G-005/36**
JAPIO CLASS: 45.9 (INFORMATION PROCESSING -- Other); 44.9 (COMMUNICATION -- Other); 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JAPIO KEYWORD: R129 (ELECTRONIC MATERIALS -- Super High Density Integrated Circuits, LSI & GS

ABSTRACT

PROBLEM TO BE SOLVED: To operate a parameter, for which the range of values to be taken is wide, at high speed with high accuracy without depending on any floating point method.

SOLUTION: The same number of bits in a mantissa part register 25 is set to a bit number register 14. When parameters (a), (b) and (c) are set to registers 11-13, the maximum value is found by a maximum value discriminator 15. A digit number computing element 16 sets the number of bits of the maximum value to a bit counter 17. Besides, the number of bits of the maximum value is compared with the fixed number of bits in the bit number register 14 and when the former number is more, its differential number (e) of bits (digits) is set to a digit number part **register** 18. Shifters 19-21 **fetch** the (a), (b) and (c) and sets a', b' and c', which are shifted to right just for the number (e) of digits, to mantissa part registers 22-24. A sum-of-products operating part 10 fetches the mantissas a', b' and c' and operates the sum of products between input values such as coordinate values X and Y, for example, as prescribed. The operated result is shifted to left just for the number (e) of digits by a digit shift part 26.

17/5/7 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

04564270 **Image available**
GRAPHIC DISPLAY CIRCUIT

PUB. NO.: 06-236170 [JP 6236170 A]
PUBLISHED: August 23, 1994 (19940823)
INVENTOR(s): ISHII HIDEAKI
APPLICANT(s): YAMATAKE HONEYWELL CO LTD [000666] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 05-041777 [JP 9341777]
FILED: February 08, 1993 (19930208)
INTL CLASS: [5] **G09G-005/02**
JAPIO CLASS: 44.9 (COMMUNICATION -- Other)
JAPIO KEYWORD: R004 (PLASMA); R011 (LIQUID CRYSTALS)
JOURNAL: Section: P, Section No. 1832, Vol. 18, No. 621, Pg. 97, November 25, 1994 (19941125)

ABSTRACT
PURPOSE: To accelerate a plotting speed.

CONSTITUTION: Mask data are decided at every bit corresponding to plotting data, and are **written** in a mask **register** 5. Further, enable/disenable data are decided at every color corresponding to the plotting data, and are **written** in a chromatic **register** 6. The preceding chromatic data are latched by latch parts 8R (8G, 8B). By bit mask circuits 7R (7G, 7B), the present chromatic data to frame memories 2R (2G, 2B) are formed based on the mask data from the mask register 5, the enable/disenable data from the chromatic register 6 and the preceding chromatic data from the latch circuits 8R (8G, 8B) while an image is processed by a CPU 1.

17/5/9 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO

04166765 **Image available**
GRAPHIC DISPLAY METHOD IN CRT DEVICE

PUB. NO.: 05-158465 [JP 5158465 A]
PUBLISHED: June 25, 1993 (19930625)
INVENTOR(s): HOSONO AKIO
APPLICANT(s): I O DATA KIKI KK [000000] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-325679 [JP 91325679]
FILED: December 10, 1991 (19911210)
INTL CLASS: [5] **G09G-005/36** ; G06F-003/14; **G09G-001/16** ; **G09G-005/34**
JAPIO CLASS: 44.9 (COMMUNICATION -- Other); 45.3 (INFORMATION PROCESSING -- Input Output Units)

JAPIO KEYWORD:R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)
JOURNAL: Section: P, Section No. 1626, Vol. 17, No. 557, Pg. 85, October 07, 1993 (19931007)

ABSTRACT

PURPOSE: To attain a high resolution display of a large amount of graphic data using a normal standard CRT device by combining the normal standard CRT and an exclusive display controller.

CONSTITUTION: The display controller is provided with a graphic memory 11, a CRT controller and shift **register** , etc. The vertical **scan** of the CRT controller can be specified for a noninterlace system or an interlace system, a screen display starting position can be specified at least in the vertical direction and a cursor control function is provided. Moreover, normal standard horizontal dots, horizontal bits whose number is larger than the number of vertical lines and a vertical bit graphic memory 11 are provided. A screen S is used to display by selecting an interlace system screen corresponding to the whole region of the memory 11 and a noninterlace system screen corresponding to a partial region. The latter screen is scrolled in the vertical direction.

17/5/11 (Item 11 from file: 347)

03061896 **Image available**

GRAPHIC DISPLAY DEVICE

PUB. NO.: 02-037396 [JP 2037396 A]
PUBLISHED: February 07, 1990 (19900207)
INVENTOR(s): IIDA SHIGERU
OHAMA TATSUYUKI
HACHIMAN MASASHI
APPLICANT(s): SANYO ELECTRIC CO LTD [000188] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-187723 [JP 88187723]
FILED: July 27, 1988 (19880727)
INTL CLASS: [5] **G09G-005/36** ; G06F-003/153; **G09G-005/02** ; G06F-015/72
JAPIO CLASS: 44.9 (COMMUNICATION -- Other); 45.3 (INFORMATION PROCESSING -- Input Output Units); 45.4 (INFORMATION PROCESSING -- Computer Applications)
JOURNAL: Section: P, Section No. 1038, Vol. 14, No. 191, Pg. 130, April 18, 1990 (19900418)

ABSTRACT

PURPOSE: To miniaturize the circuit by decreasing the number of connecting lines and elements by providing plural coincidence circuits for detecting the coincidence of each bit output of parallel data which have been read out to a data bus by a control circuit and a 1-bit output of picture element data.

CONSTITUTION: Picture element data of plural bits for showing a designated color or gradation is set to a **register** 10, and when a **read** -out request is issued once from a CPU 1, a plane component of an (m) picture element portion is read out to data buses 5, 6 by a time division, respectively from a graphic memory 2, and in (m) pieces of coincidence circuits 1700-1715, the coincidence with each plane component of picture element data which has been set to the register 10 is detected by a time division at every plane. In this state, if a component which does not coincide exists even one among all the plane components, in holding circuits 1900-1915 of the (m)-picture element portion, a result of discrepancy is held in the holding circuit corresponding to its picture element. In such a way, the number of connecting lines and the number of coincidence circuits are decreased, and the circuit can be miniaturized.

17/5/12 (Item 12 from file: 347)
DIALOG(R)File 347:JAPIO

02287431 **Image available**
GRAPHIC DISPLAY DEVICE

PUB. NO.: 62-204331 [JP 62204331 A]
PUBLISHED: September 09, 1987 (19870909)
INVENTOR(s): TERADA HIDEFUMI
MORIMOTO MINORU
OMORI MUTSUHIRO
APPLICANT(s): NIPPON GAKKI SEIZO KK [000407] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-046673 [JP 8646673]
FILED: March 04, 1986 (19860304)
INTL CLASS: [4] G06F-003/153; **G09G-001/16**
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 44.9 (COMMUNICATION -- Other)
JOURNAL: Section: P, Section No. 670, Vol. 12, No. 62, Pg. 77, February 25, 1988 (19880225)

ABSTRACT

PURPOSE: To reduce a memory or circuit quantity by using a clipping means to process a part of picking processing.

CONSTITUTION: A single point is indicated by a light pen on a pattern C and the coordinates of said point are supplied. A CPU decides a small area including the input coordinates, i.e., a picking area 52. Then both minimum and maximum coordinates Xl, Xh, Yl and Yh in X and Y directions of the area 52 respectively are set by the CPU at four **registers** 46-49 in a clipping **checker** 38. The patterns A, B, C... are successively drawn again and a picking flag 51 is checked every time the drawing is through with a pattern. Here a point on the pattern C passes through the area 52, therefore the flag 51 is turned on after the pattern C is drawn by the function of the checker 38. In such a way, the selected pattern C is detected and the prescribed processing is applied to this pattern C.

17/5/13 (Item 13 from file: 347)
DIALOG(R)File 347:JAPIO

01389347 **Image available**
GRAPHIC DISPLAY DEVICE

PUB. NO.: 59-100947 [JP 59100947 A]
PUBLISHED: June 11, 1984 (19840611)
INVENTOR(s): HIRATA HITOSHI
APPLICANT(s): PIONEER ELECTRONIC CORP [000501] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 57-209234 [JP 82209234]
FILED: December 01, 1982 (19821201)
INTL CLASS: [3] G06F-003/037; G06F-003/14; **G09G-003/20**
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 44.9 (COMMUNICATION -- Other)
JAPIO KEYWORD: R004 (PLASMA); R116 (ELECTRONIC MATERIALS -- Light Emitting Diodes, LED); R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)
JOURNAL: Section: P, Section No. 306, Vol. 08, No. 219, Pg. 5, October 05, 1984 (19841005)

ABSTRACT

PURPOSE: To attain simply a **graphic display** by means of human fingers, a light pen, etc. with high operability by displaying the static electricity or a signal of induced hum, etc. applied through a matrix by a microprocessor on a liquid crystal device.

CONSTITUTION: When the surface of a matrix 2 is traced with a light pen P, the static electricity is applied to signal lines 2a and 2b. Then the signals are supplied to wave detectors 4 and 7 through multiplexers 3 and 6. Furthermore the detected signals are supplied to registers 10a and 10b through latch circuits 5 and 8. A controller 10c **reads** the signals supplied from **registers** 10a and 10b and stops temporarily the address outputs of X and Y directions. The position traced by the pen P on the matrix 2 is calculated based on the addresses of X and Y directions and stored in a memory 10d, and the multiplexers 3 and 6 are swept by the address outputs of X and Y directions supplied from the controller 10c. The position information on the matrix 2 traced by the pen P and stored in the memory 10d is successively delivered to a driver 11a for liquid crystal.

17/5/14 (Item 14 from file: 347)
DIALOG(R)File 347:JAPIO

01134843 **Image available**
HIGH SPEED **GRAPHIC DISPLAY** SYSTEM

PUB. NO.: 58-072243 [JP 58072243 A]
PUBLISHED: April 30, 1983 (19830430)
INVENTOR(s): SUZUKI YASUHIRO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-169770 [JP 81169770]
FILED: October 23, 1981 (19811023)
INTL CLASS: [3] G06F-003/14; **G09G-001/00**
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 44.9 (COMMUNICATION -- Other)
JOURNAL: Section: P, Section No. 211, Vol. 07, No. 164, Pg. 139, July 19, 1983 (19830719)

ABSTRACT

PURPOSE: To register and discriminate graphic data at high speed by using two displaying areas and one registering area for the graphic data to process the generation and display of the graphic data concurrently.
CONSTITUTION: An IC block, a net and an IC pin are stored in a shape definition data 1 in every logic unit. A generation/writing part 2 writes a graphic data of the IC block in a writing area 4 for display. A display part 8 transfers the data written in the area 4 to a **graphic display** device 10 to draw an IC block picture on its screen. The IC block data in displaying are registered in an **writing** area 7 for **register** and net graphic data are **written** in a writing area 5. After completing the display of the IC block, the net in the area 5 is displayed. During the net display, the net graphic data are registered in the area 7, the contents of the area 4 are cleared and the IC pin is written in the area 4. Thus the contents of the area 7 are transferred when a **graphic** on the **screen** is once cleared and the same screen is displayed again.

17/5/44 (Item 30 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003872536
WPI Acc No: 1984-018067/198404
XRPX Acc No: N84-013474
Graphics display **control for VDU - allows symbols and figures to be readily moved to new location**
Patent Assignee: SIEMENS AG (SIEI)
Inventor: ZIEGLER B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3223482	A	19840112	DE 3223482	A	19820623	198404	B

Priority Applications (No Type Date): DE 3223482 A 19820623
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
DE 3223482 A 12

Abstract (Basic): DE 3223482 A
The monitor receives control signals from a cathode ray control unit via a video signal generator. Units controlling the form of the display are linked by a common data bus and address. A display memory is **accessed** by an address multiplex **register** such that each screen point is represented by a memory cell. The memory contains two regions, one for status signals and the other figure identify signals.S The system operates with figure identifying signal comparator and a figure change circuit. In the event of coincidence between values the stored data is modified to allow only that specific figure to be adjusted in position on the screen.
0/1
Title Terms: GRAPHIC; DISPLAY; CONTROL; VDU; ALLOW; SYMBOL; FIGURE; READY; MOVE; NEW; LOCATE
Derwent Class: P85; T01; T04
International Patent Class (Additional): G06F-003/15; **G09G-001/02**
File Segment: EPI; EngPI

17/5/46 (Item 32 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003758787
WPI Acc No: 1983-754998/198336
XRPX Acc No: N83-156693
CAD **video display system - uses memory for storing set of symbol fragments with control circuitry allowing symbol or fragments to appear in one of four orientations**
Patent Assignee: DAISY SYST CORP (DAIS-N)
Inventor: FINEGOLD A
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2115658	A	19830907	GB 8230542	A	19821026	198336	B
US 4533911	A	19850806	US 82351647	A	19820224	198534	
GB 2115658	B	19860108				198602	

Priority Applications (No Type Date): US 82351647 A 19820224
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
GB 2115658 A 10

Abstract (Basic): GB 2115658 A
In a display system, codes for symbols or fragments thereof are generated by computer, loaded (21) into a buffer (20) holding sufficient data for a page, and thence loaded into alternately used row buffers (24). Each code comprises the address in RAM or ROM (25) of the stored symbol pattern, together with four bits indicating vertical and lateral inversion, black-white interchange and blinking display. Successive codes from the row buffer (24) are read out into the symbol memory (25), from which the corresponding 7 x 7 matrix patterns of pixels are **read** line by line into shift **register** (35) and into filters (26) and (36).
Filter (26) determines whether the top or bottom line is read first, filter (36) determines whether the first or last pixel of each line is **read** out of shift **register** (35) to the parallel/serial converting register (40). Filter (37) then establishes video black or white and blinking display where coded. Each symbol or fragment can therefore appear with one of four orientations to build up complex diagrams or rotation on the display raster.
1/8
Title Terms: **CAD** ; VIDEO; DISPLAY; SYSTEM; MEMORY; STORAGE; SET; SYMBOL;

FRAGMENT; CONTROL; CIRCUIT; ALLOW; SYMBOL; FRAGMENT; APPEAR; ONE; FOUR; ORIENT
Index Terms/Additional Words: COMPUTER; AID; DESIGN
Derwent Class: P85; T01; T04
International Patent Class (Additional): G06F-003/15; G06F-015/66; **G09G-001/16**
File Segment: EPI; EngPI

17/5/47 (Item 33 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003713654
WPI Acc No: 1983-709837/198328
XRPX Acc No: N83-121916
CRT graphic **data** display **device - has output from interface unit fed to control unit and to storage directly, and via register commutator counter and decoder**
Patent Assignee: AS UKR CYBERNETICS (AUCY)
Inventor: DOMBRUGOV V R; GOLUBCHIK V Y; SIVERSKII P M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
SU 955180	A	19820902				198328 B

Priority Applications (No Type Date): SU 2911442 A 19800310
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
SU 955180	A		5		

Abstract (Basic): SU 955180 A
The CRT **graphic** data **display** device allows scan length of each graphic to be varied independently since, in addition to interface unit (1), control unit (2), storage unit (3), code-time converter (4), and television receiver (5) with control unit (6) and CRT (7), the device also has extra registers (8,10), commutator (9), counter (11), and decoder (12).
For each graphic, control unit (2) computes corresponding addresses for storage unit (3) and registers (8,10). Contents of register (10), representing tone before new graphic coordinates can be read into storage (3), is read to counter (11), and decreased by regular clock-pulses. If counter (11) contents is non-zero, no graphic is written to storage (3), and counter (11) contents is fed via commutator (9) to register (10). When counter (11) equals zero, graphic is fed to storage (3), and division coefficient code is **read** from **register** (8) via commutator (9) to register (10). Bul. 32/30.8.82. (5pp Dwg.No.1/3)
Title Terms: CRT; GRAPHIC; DATA; DISPLAY; DEVICE; OUTPUT; INTERFACE; UNIT; FEED; CONTROL; UNIT; STORAGE; REGISTER; COMMUTATE; COUNTER; DECODE
Derwent Class: P85; T01; T04
International Patent Class (Additional): **G09G-001/06**
File Segment: EPI; EngPI

17/5/49 (Item 35 from file: 350)
DIALOG(R)File 350:Derwent WPIX

002133857
WPI Acc No: 1979-F3789B/197925
Coloured graphical **character** display **- is for mixed colour cells of video display screen and uses colour and character registers**
Patent Assignee: IBM CORP (IBMC)
Inventor: ROE D; SOWTER B R
Number of Countries: 006 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week

DE 2851772	A	19790613	197925	B
FR 2411446	A	19790810	197938	
US 4217577	A	19800812	198035	
GB 1593309	A	19810715	198129	
CA 1104730	A	19810707	198136	
DE 2851772	C	19850117	198504	
IT 1160275	B	19870311	198918	

Priority Applications (No Type Date): GB 7751441 A 19771209

Abstract (Basic): DE 2851772 A

The device is for displaying coloured graphical characters on a display unit screen divided into image cells enables colour mixing in individual cells to be achieved cheaply and economically. A character store contains one or more character sets in character video cells corresp. to image cells (C1, C2, C3). Data corresp. to characters are stored in an image register.

Video data corresp. to colour components are extracted from colour registers synchronised with the display unit. A controller forms video data for cells (8) from the data **read** from the image **register** by transferring character video cells to the colour registers.

Title Terms: COLOUR; GRAPHICAL; CHARACTER; DISPLAY; MIX; COLOUR; CELL; VIDEO; DISPLAY; SCREEN; COLOUR; CHARACTER; REGISTER

Derwent Class: P85; T01; T04; U14

International Patent Class (Additional): G06F-003/14; G06K-015/20; G09F-003/00; **G09G-001/16** ; G09X-000/00; G11C-008/00; H01S-003/22; H04N-000/00

File Segment: EPI; EngPI

20/5/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014844874 **Image available**
WPI Acc No: 2002-665580/200271
XRPX Acc No: N02-526556
Device controller for computer system, has processor for writing device performance state that is read from status register through interface, in control register
Patent Assignee: CLINE L E (CLIN-I); GEORGE V (GEOR-I); WYATT D (WYAT-I)
Inventor: CLINE L E; GEORGE V; WYATT D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020087897	A1	20020704	US 2000751530	A	20001229	200271	B

Priority Applications (No Type Date): US 2000751530 A 20001229
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020087897	A1		10	G05B-011/01	

Abstract (Basic): US 20020087897 A1
NOVELTY - A processor writes device performance state that is **read** from a status **register** (15) through an interface, in a control register (16).
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(1) Device performance state control method;
(2) Device performance state control system; and
(3) Machine-readable medium storing program for controlling device performance state.
USE - For monitoring and controlling individual device performance states of multiple devices such as disk drive, display device, modem, **graphics** accelerator, network **interface** and keyboard in computer system.
ADVANTAGE - Controls performance states of devices effectively, and permits integrated power management of all the devices at the system level.
DESCRIPTION OF DRAWING(S) - The figure shows the device controller for computer system.
Status register (15)
Control register (16)
pp; 10 DwgNo 1/4
Title Terms: DEVICE; CONTROL; COMPUTER; SYSTEM; PROCESSOR; WRITING; DEVICE; PERFORMANCE; STATE; READ; STATUS; REGISTER; THROUGH; INTERFACE; CONTROL; REGISTER
Derwent Class: T01; T06; U21
International Patent Class (Main): G05B-011/01
International Patent Class (Additional): G05B-009/02; G06F-001/26; G06F-001/28; G06F-001/30; G06F-009/00
File Segment: EPI

20/5/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014507560 **Image available**
WPI Acc No: 2002-328263/200236
XRPX Acc No: N02-257531
Large scale integrated chip layout design method using CAD , involves arranging boundary scan registers in empty regions near target input/output cells, and adjusting fan-out of the boundary scan registers
Patent Assignee: FUJITSU LTD (FUIT); ABE K (ABEK-I); OSAKI S (OSAK-I)
Inventor: ABE K; OSAKI S
Number of Countries: 002 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020004929	A1	20020110	US 2001789490	A	20010222	200236	B
JP 2002026129	A	20020125	JP 2000202479	A	20000704	200236	
US 6564362	B2	20030513	US 2001789490	A	20010222	200335	

Priority Applications (No Type Date): JP 2000202479 A 20000704
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020004929	A1		20	G06F-017/50	
JP 2002026129	A		12	H01L-021/82	
US 6564362	B2			G06F-017/50	

Abstract (Basic): US 20020004929 A1

NOVELTY - The input/output connection boundary **scan registers** are arranged in empty regions near target input/output cells. The output input/output control boundary **scan registers** are arranged, based on arrangement positions of target input/output connection boundary **scan registers** . The fan-out of **registers** , is adjusted.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for computer-readable medium storing LSI chip layout designing program.

USE - For designing layout of LSI chip using **CAD** .

ADVANTAGE - Since the arrangement of registers and fan-out adjustment are done automatically, man-hour for LSI development is greatly reduced. The fan-out adjustment is done with minimum number of buffer cells, thus resulting in elimination of crossing of nets of test signals to boundary **scan registers** .

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart explaining LSI chip layout designing process.

pp; 20 DwgNo 2/13

Title Terms: SCALE; INTEGRATE; CHIP; LAYOUT; DESIGN; METHOD; **CAD** ; ARRANGE ; BOUNDARY; SCAN; REGISTER; EMPTY; REGION; TARGET; INPUT; OUTPUT; CELL; ADJUST; FAN; BOUNDARY; SCAN; REGISTER
Derwent Class: T01; U11; U13
International Patent Class (Main): G06F-017/50; H01L-021/82
International Patent Class (Additional): H01L-021/822; H01L-027/04
File Segment: EPI

20/5/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011624494 **Image available**
WPI Acc No: 1998-041622/199804
Related WPI Acc No: 1996-277293
XRPX Acc No: N98-033419

Register access control for CAD , pattern or graphic drawing utilisation device - uses multiplexer controlled by flag to disconnect registers from bus to inhibit CPU from accessing registers and allow command executing unit to access registers

Patent Assignee: NEC CORP (NIDE)
Inventor: MATSUDA N
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5696992	A	19971209	US 9359763	A	19930512	199804	B
			US 96644276	A	19960510		

Priority Applications (No Type Date): JP 92118655 A 19920512
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5696992	A		16	G06F-015/16	Div ex application US 9359763
					Div ex patent US 5524260

Abstract (Basic): US 5696992 A

While a busy state is indicated in a status register by a first busy signal kept active while a command is stored in a parameter

register group as a stored command, a free state is indicated while a second busy signal is kept inactive until later kept active while a parameter group is stored in the parameter register group as a stored parameter group. After lapse of the free state during which a command executing unit is operable without reference to the stored parameter group, the unit is operable by using a working register group alone.

A like parameter group can be stored in the parameter register group, which is connected to a bus through a multiplexer while the second busy signal is inactive. During a short interval during which the first busy signal is inactive and before the second busy signal is activated, another command can be stored through the multiplexer. A logic circuit can be used instead of the status register.

ADVANTAGE - Provides short waiting time in putting utilisation device in correct operation. Merits of parallel operation of information processing system and graphic drawing device are not adversely affected.

Dwg.4/9

Title Terms: REGISTER; ACCESS; CONTROL; **CAD** ; PATTERN; GRAPHIC; DRAW; UTILISE; DEVICE; MULTIPLEX; CONTROL; FLAG; DISCONNECT; REGISTER; BUS; INHIBIT; CPU; ACCESS; REGISTER; ALLOW; COMMAND; EXECUTE; UNIT; ACCESS; REGISTER

Derwent Class: T01

International Patent Class (Main): G06F-015/16

File Segment: EPI

20/5/13 (Item 13 from file: 350)

DIALOG(R)File 350:Derwent WPIX

011109065 **Image available**

WPI Acc No: 1997-086990/199708

Related WPI Acc No: 1994-151533; 1997-132168; 1997-280623; 1997-402147; 1998-583078

XRPX Acc No: N97-071742

Local Bus Peripheral Interface between computer and Winchester hard disk drive or colour graphics display **- has pipelined architecture which includes Read Ahead Buffer, Read Ahead Counter, Data Out Latch, and Controlling State Machine with** Configuration Register **, and couples on host side to either VL bus or PCI bus**

Patent Assignee: CIRRUS LOGIC INC (CIRR-N)

Inventor: CHEJLAVA E J; CLINE L E; CURT K C

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5592682	A	19970107	US 92964590	A	19921020	199708	B
			US 94329557	A	19941025		

Priority Applications (No Type Date): US 94329557 A 19941025; US 92964590 A 19921020

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5592682	A		46	G06F-015/02	CIP of application US 92964590

Abstract (Basic): US 5592682 A

The high performance Local Bus Peripheral Interface (LBPI) is coupled between the computer local bus and the peripheral interface(s), and has a pipelined architecture which includes a Read Ahead Buffer, a Read Ahead Counter, a Data Out Latch, and a Controlling State Machine with a **Configuration Register** .

The LBPI can be selectably configured to couple on the host side to either a VL bus or PCI bus. Efficiency of Read-Ahead operations is further enhanced by maintaining a count down of the number of words of a data sector already transferred and/or snooping the peripheral device commands from the computer to intelligently predict the occurrence of subsequent read data transfers commands. The Controlling State Machine also snoops the peripheral device commands to maintain its record of the operating parameters of the peripheral devices and also keeps track

of which of the devices is currently active.

The LBPI supports DMA and PIO data transfers on the peripheral side, or alternatively, the LBPI translates memory data transfers into I-O data transfers to improve efficiency of I-O data transfers. A DMA Time-out Counter is used during DMA mode data transfer operations to prevent the system from indefinitely waiting for an appropriate DMA Request Signal from a selected peripheral. During a DMA mode data transfer operation, forced interrupts may be generated and transmitted to the host in order to emulate a PIO mode data transfer operation. During a DMA mode data transfer operation, an imposed status or Fake 3F6 register is used to transmit status information to the host system.

ADVANTAGE - High performance Local Bus Peripheral Interface (LBPI) for computer local bus and high performance peripheral interfaces, using pipelined architecture. Increases use of available data transfer bandwidth.

Dwg.7/23

Title Terms: LOCAL; BUS; PERIPHERAL; INTERFACE; COMPUTER; WINCHESTER; HARD; DISC; DRIVE; COLOUR; GRAPHIC; DISPLAY; PIPE; ARCHITECTURE; READ; AHEAD; BUFFER; READ; AHEAD; COUNTER; DATA; LATCH; CONTROL; STATE; MACHINE; CONFIGURATION; REGISTER; COUPLE; HOST; SIDE; BUS; BUS

Derwent Class: T01

International Patent Class (Main): G06F-015/02

File Segment: EPI

20/5/17 (Item 17 from file: 350)

010444938 **Image available**

WPI Acc No: 1995-346255/199545

XRPX Acc No: N95-258878

Power management unit for computer system - allows computer system to be specified through software using configuration **and index** registers

Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)

Inventor: OBRIEN R M; WISOR M; O'BRIEN R M; WISOR M T

Number of Countries: 016 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 676687	A2	19951011	EP 95301742	A	19950316	199545	B
JP 7295693	A	19951110	JP 9580452	A	19950405	199603	
EP 676687	A3	19960605	EP 95301742	A	19950316	199632	
US 6021498	A	20000201	US 94223770	A	19940406	200013	
EP 676687	B1	20000913	EP 95301742	A	19950316	200046	
DE 69518781	E	20001019	DE 618781	A	19950316	200060	
			EP 95301742	A	19950316		

Priority Applications (No Type Date): US 94223770 A 19940406

Cited Patents: No-SR.Pub; 2.Jnl.Ref; US 5129068

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 676687	A2	E	8	G06F-001/26	
Designated States (Regional): AT BE DE DK ES FR GB GR IE IT LU NL PT SE					
JP 7295693	A		1	G06F-001/26	
EP 676687	A3			G06F-001/26	
US 6021498	A			G06F-001/00	
EP 676687	B1	E		G06F-001/26	
Designated States (Regional): AT BE DE DK ES FR GB GR IE IT LU NL PT SE					
DE 69518781	E			G06F-001/26	Based on patent EP 676687

Abstract (Basic): EP 676687 A

The unit includes several **configuration registers** which store information used in setting a mode of operation. An index decoder is coupled to each of the registers, so as to enable one of them. An index register is coupled to the index decoder. It stores an index value which determines the register to be enabled.

A programme register stores a value which sets an address location

of the index register. A control unit is coupled to the programme register and the index register. The control unit latches an index value within the index **register** in response to a **write** cycle to the address location.

USE/ADVANTAGE - For **computer aided design** . Reduced size of control unit. Flexible.

Dwg.1/2

Title Terms: POWER; MANAGEMENT; UNIT; COMPUTER; SYSTEM; ALLOW; COMPUTER; SYSTEM; SPECIFIED; THROUGH; SOFTWARE; CONFIGURATION; INDEX; REGISTER
Derwent Class: T01
International Patent Class (Main): G06F-001/00) 06F-001/26
International Patent Class (Additional): G06F-009/35; G06F-013/14
File Segment: EPI

20/5/19 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009172207 **Image available**
WPI Acc No: 1992-299641/199236
Related WPI Acc No: 1993-320296; 1997-549214
XRPX Acc No: N92-229516

Data processor with self-emulation capability for graphics processing - has arithmetic logic unit, register, emulation control terminal and stop, load and pump circuits controlling register writing **operations**

Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: ASAL M; DYE T A; GUTTAG K M; ROSKELL D; SIMPSON R; TEBBUTT N; VAN AKEN J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5140687	A	19920818	US 85790299	A	19851022	199236 B
			US 86948337	A	19861231	
			US 89415375	A	19890927	

Priority Applications (No Type Date): US 86948337 A 19861231; US 85790299 A 19851022; US 89415375 A 19890927
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5140687	A		37	G06F-015/62	CIP of application US 85790299 Cont of application US 86948337

Abstract (Basic): US 5140687 A

The processing appts. uses a register having a number of control and data terminals. The emulation control terminal receives an emulation control siganl having logic states. The stop circuit is connected to the emulation control terminal and arithmetic logic unit for stopping execution of instructions by the ALU in response to the emulation control signal being at its first logic state. The stop circuit enables execution of instructions by the arithmetic logic unit in response to the emulation control signal being at its second logic states.

The dumping circuit is responsive to the stop circuit stopping execution by the ALU and a dump siganl applied to one of the control terminals for **writing** the contents of the **register** to the data terminals. The loading circuit is responsive to the stop circuit stopping execution and to a load signal applied to one of the control terminals for **writing** to the **register** the value of a digital signal applied to the data terminals.

USE - Bit mapped computer **graphics** processing. **Software** development using emulation function.

Dwg.2/21

Title Terms: DATA; PROCESSOR; SELF; EMULATION; CAPABLE; GRAPHIC; PROCESS; ARITHMETIC; LOGIC; UNIT; REGISTER; EMULATION; CONTROL; TERMINAL; STOP; LOAD; PUMP; CIRCUIT; CONTROL; REGISTER; WRITING; OPERATE
Derwent Class: T01
International Patent Class (Main): G06F-015/62

24/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

02403645 **Image available**
REGISTER READ -OUT DEVICE FOR **EMULATOR**

PUB. NO.: 63-020545 [JP 63020545 A]
PUBLISHED: January 28, 1988 (19880128)
INVENTOR(s): HIRATSUKA YASUTETSU
APPLICANT(s): YOKOGAWA HEWLETT PACKARD LTD [355232] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-164896 [JP 86164896]
FILED: July 14, 1986 (19860714)
INTL CLASS: [4] G06F-011/28; G06F-011/22
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)
JOURNAL: Section: P, Section No. 722, Vol. 12, No. 226, Pg. 91, June 28, 1988 (19880628)

ABSTRACT

PURPOSE: To read out the contents of a write only register by using an **emulator** , by constituting the titled device so that a write data is written in response to an output of the first decoder, and the stored contents are read out in response to an output of the second decoder.

CONSTITUTION: The second decoder 104 in a register reading-out circuit 243 sets an output 114 to a high level, when a read-out access is executed to some specific address Ab being different from an address A of a register R, in a background state. Accordingly, when a monitor running on a microprocessor 245 executes a read-out access to this address Ab, a data in a register 106, namely, a data which has been written in a write only register R recently is read out. This data is displayed on a CRT display, etc. provided on a host. In this way, in case a user program executes an access to a usual memory, the register 106 is invisible, and the access is executed to a usual memory, therefore, an address used by the user program is not limited

24/5/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014964598 **Image available**
WPI Acc No: 2003-025112/200302
XRPX Acc No: N03-020136
Register control apparatus for in-circuit emulator **, decodes input serial data using instruction code, based on which input data is connected to** register **or to boundary** scan register
Patent Assignee: FUJITSU LTD (FUIT)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2002328152	A	20021115	JP 2001133674	A	20010427	200302	B

Priority Applications (No Type Date): JP 2001133674 A 20010427
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2002328152	A		14	G01R-031/28	

Abstract (Basic): JP 2002328152 A
NOVELTY - A serial input terminal (3) receives the serial input data which is decoded using an instruction code. A control signal generating unit generates a data control signal based on the decoded input, for accordingly connecting the input data to the register (2) or to a boundary scan register (BSR) (13), for controlling the register (2) of the in-circuit **emulator** (ICE).

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(1) Register controlling method; and
(2) Register control system.
USE - For controlling register in in-circuit **emulator** (ICE) that uses join test action group (JTAG) interface.
ADVANTAGE - The serial input data received from a user is decoded to generate the register control signal for controlling the **emulator** register, therefore private commands can be received from user freely, thus the problem of lack of private commands is solved.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the register control system. (Drawing includes non-English language text).
Register (2)
Serial input terminal (3)
Boundary scan register (13)
pp; 14 DwgNo 1/10

Title Terms: REGISTER; CONTROL; APPARATUS; CIRCUIT; **EMULATION** ; DECODE; INPUT; SERIAL; DATA; INSTRUCTION; CODE; BASED; INPUT; DATA; CONNECT; REGISTER; BOUNDARY; SCAN; REGISTER
Derwent Class: S01; T01
International Patent Class (Main): G01R-031/28
International Patent Class (Additional): G06F-011/22; G06F-015/78
File Segment: EPI

24/5/7 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014368771 **Image available**
WPI Acc No: 2002-189473/200225
XRPX Acc No: N02-143586
Simulator **has PCI bus through which result of** simulation **execution performed based on control information in** registers **of** simulator acquired **from** register , **is transmitted to** registers **by control CPU**
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: OTSUKA T
Number of Countries: 028 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1134638	A2	20010919	EP 2001106046	A	20010312	200225 B
US 20010025235	A1	20010927	US 2001804302	A	20010313	200225
JP 2001331346	A	20011130	JP 200148497	A	20010223	200225

Priority Applications (No Type Date): JP 200069232 A 20000313
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1134638	A2	E	30	G05B-019/418	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR				
US 20010025235	A1			G06F-009/44	
JP 2001331346	A		18	G06F-011/28	

Abstract (Basic): EP 1134638 A2
NOVELTY - The **simulator** has registers (114a) connected to a control CPU (113) and a **simulation** CPU (115). The **simulation** CPU acquires control information written into the registers through the PCI bus (116). The control CPU transmits the execution of **simulation** performed based on acquired control information to the registers through the bus.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) **Simulation** method;
(b) **Simulation** system
USE - **Simulator** .
ADVANTAGE - The operation of the real machine is monitored and **simulation** is executed in synchronization with the operation of real

machine. As the **simulation** execution result is stored in the registers, program for operating the real machine is executed with less modifications.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of **simulator** .

Control CPU (113)

Registers (114a)

Simulation CPU (115)

PCI bus (116)

pp; 30 DwgNo 2/14

Title Terms: **SIMULATE** ; BUS; THROUGH; RESULT; **SIMULATE** ; EXECUTE; PERFORMANCE; BASED; CONTROL; INFORMATION; REGISTER; **SIMULATE** ; ACQUIRE; REGISTER; TRANSMIT; REGISTER; CONTROL; CPU

Derwent Class: T01; T06

International Patent Class (Main): G05B-019/418; G06F-009/44; G06F-011/28

File Segment: EPI

24/5/19 (Item 18 from file: 350)

DIALOG(R)File 350:Derwent WPIX

012089284 **Image available**

WPI Acc No: 1998-506195/199843

Related WPI Acc No: 1996-068584; 1997-549314; 2000-636986

XRPX Acc No: N98-394650

Dual instruction set CPU - accesses **SRRO** register **loaded based on input** emulation **code, using RISC supervisor code**

Patent Assignee: S3 INC (STHR-N)

Inventor: BLOMGREN J S; RICHTER D E

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5805918	A	19980908	US 94277962	A	19940720	199843 B
			US 95547395	A	19951024	

Priority Applications (No Type Date): US 94277962 A 19940720; US 95547395 A 19951024

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5805918	A		14	G06F-009/30	Cont of application US 94277962 Cont of patent US 5481693

Abstract (Basic): US 5805918 A

The CPU has CISC EFLAGS register and RISC CR register which are combined to a single 32bitCR/EFLAGS register (40) accessed by CISC user programs and RISC user programs and an **emulation** code. The CISC code segment base address register and RISC count CTR register are combined to a single CS/CTR register (40). The RISC system save/restore (SRRO) register holds the address to return to, after processing an interruption. The SRRO also holds a RISC or CISC address. When the **emulation** code is input, the SRRO register (44) is loaded, by the user.

The register is accessed using RISC supervisor code and **emulation** code. The merged FP-IP/LR register (46) is indirectly accessed by CISC programs. The 32 general purpose registers from RISC are combined with 8GPR and 6segment base registers from CISR are merged with 48GPR.

ADVANTAGE - Avoids interference between two instruction sets in shared registers. Improves floating point processing efficiency.

Dwg.3,4/4

Title Terms: DUAL; INSTRUCTION; SET; CPU; ACCESS; REGISTER; LOAD; BASED; INPUT; **EMULATION** ; CODE; SUPERVISION; CODE

Derwent Class: T01

International Patent Class (Main): G06F-009/30

File Segment: EPI

24/5/26 (Item 25 from file: 350)

DIALOG(R)File 350:Derwent WPIX

010667284 **Image available**
WPI Acc No: 1996-164238/199617
XRPX Acc No: N96-137781
Simulator **for debugging software program - includes** simulation **register to set succeeding address value of tested program** read **from address information** register
Patent Assignee: NIPPON DENKI TSUSHIN SYSTEM KK (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8044591	A	19960216	JP 94176365	A	19940728	199617	B

Priority Applications (No Type Date): JP 94176365 A 19940728
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8044591	A		8	G06F-011/28	

Abstract (Basic): JP 8044591 A
The **simulator** has a **simulation** controller (2a). An address registration device (3) registers the head address of the message processing program. An address comparison device (5) compares the registered header address and the address of the machine language instruction read by a program reading control device (6a).
The reading of machine language address is detected, and it is reported to the **simulation** control device. The message interrupted by the **simulation** process and stored in a message storing device (8), is output. A command analysis execution device (7a) extracts and stores the succeeding address of the message portion in a **simulation** address register (13).
ADVANTAGE - Shortens **simulation** time. Improves debugging efficiency.
Dwg.1/2
Title Terms: **SIMULATE** ; DEBUG; SOFTWARE; PROGRAM; **SIMULATE** ; REGISTER; SET; SUCCEEDING; ADDRESS; VALUE; TEST; PROGRAM; READ; ADDRESS; INFORMATION; REGISTER
Derwent Class: T01
International Patent Class (Main): G06F-011/28
File Segment: EPI

24/5/41 (Item 40 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007629187 **Image available**
WPI Acc No: 1988-263119/198837
XRPX Acc No: N88-199595
Computer-peripheral interface - enters emulated **code of symbol by** reading **data in input state** register **address standard cycle**
Patent Assignee: KULAKOV M G (KULA-I)
Inventor: KULAKOV M G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
SU 1377864	A	19880229	SU 4101677	A	19860610	198837	B

Priority Applications (No Type Date): SU 4101677 A 19860610
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
SU 1377864	A		16		

Abstract (Basic): SU 1377864 A
Appts. comprises control inputs (1,2), computer rail (3), control signals decoder (4), channel transceivers (5), address decoder (6), channel receiver (7), NOT-gates (8,9), data multiplexer (10), trigger (11), selector (12), OR-gates (13,17,26,27), 01D gates (14,19,24),

triggers (15,16), shift register (18), trigger (2[redacted], counter (21), selector (22), encoder (23), counter (25), selector (28), delay element (29), and restart blocking unit (30).

Automatic execution of special computer restart programmes is now enabled for protection against critical situations by the introduction of two OR-gates, channel receivers, two NOT-gates, four triggers, shift register, two counters. When the unit switches from programmed working to communications with the terminal, the unit realises a sequence of operations, when the carriage return symbol codes are output, lines are transferred, the next command address codes terminal is passed to the terminal, the carriage return command is executed again and the symbol code is issued.

USE/ADVANTAGE - Appts. may be used for the execution of special programmes e.g. for evaluating restart of a computer from a control terminal. Bul.8/29.2.88.

1/7

Title Terms: COMPUTER; PERIPHERAL; INTERFACE; ENTER; **EMULATION** ; CODE; SYMBOL; READ; DATA; INPUT; STATE; REGISTER; ADDRESS; STANDARD; CYCLE
Derwent Class: T01
International Patent Class (Additional): G06F-013/00
File Segment: EPI

24/5/43 (Item 42 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007079772
WPI Acc No: 1987-079769/198711
XRPX Acc No: N87-060309

Data processing system for virtual command emulator **- has circuit which receives pre-fetched command from memory, decodes to determine address of index** register **and** fetches register **contents**

Patent Assignee: NCR CORP (NATC)
Inventor: CHAN K K; NGUYEN T D; PATEL C R
Number of Countries: 006 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8701482	A	19870312	WO 86US1712	A	19860821	198711	B
EP 235255	A	19870909	EP 86905533	A	19860821	198736	
US 4722047	A	19880126	US 85770459	A	19850829	198807	
JP 63500688	W	19880310	JP 86504685	A	19860821	198816	
CA 1260618	A	19890926				198944	
EP 235255	B	19900711				199028	
DE 3672605	G	19900816				199034	

Priority Applications (No Type Date): US 85770459 A 19850829
Cited Patents: EP 10188; EP 117655; GB 2047928; US 3504349; WO 8300241
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8701482	A	E	43		
Designated States (National): JP					
Designated States (Regional): DE FR GB					
EP 235255	A	E			
Designated States (Regional): DE FR GB					
US 4722047	A		18		
EP 235255	B				
Designated States (Regional): DE FR GB					

Abstract (Basic): WO 8701482 A

The prefetch circuit includes a storage buffer (204) for receiving a command from a memory (14) and a decoder. The command is decoded to determine the address of an index register identified in the command for fetching the contents of the register. The prefetch circuit also includes virtual and real address storage registers (221,224) for receiving and storing the addresses of the command. A predetermined offset to the virtual and real addresses is added (236) to obtain new virtual and real addresses.

A comparator (240) determines if the new virtual address from the adder (236) has crossed a virtual page boundary. A transfer circuit responsive to the comparator (214) sends the real address from the storage register (224) to the adder (236) for adding the offset. Thus a new real address is obtained. The circuit then refetches a command from the memory (14) at the new real address. The storage buffer (204) also includes registers for storing prefetched data and a prefetched index register.

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Title Terms: DATA; PROCESS; SYSTEM; VIRTUAL; COMMAND; **EMULATION** ; CIRCUIT; RECEIVE; PRE; COMMAND; MEMORY; DECODE; DETERMINE; ADDRESS; INDEX; REGISTER; REGISTER; CONTENT

Derwent Class: T01

International Patent Class (Additional): G06F-009/38; G06F-012/02

File Segment: EPI

```
File   8:Ei Compendex(R) 1970-2003/Jul W3
         (c) 2003 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2003/Jun
         (c) 2003 ProQuest Info&Learning
File 202:Info. Sci. & Tech. Abs. 1966-2003/Jun 30
         (c) Information Today, Inc
File  65:Inside Conferences 1993-2003/Jul W4
         (c) 2003 BLDSC all rts. reserv.
File   2:INSPEC 1969-2003/Jul W3
         (c) 2003 Institution of Electrical Engineers
File 233:Internet & Personal Comp. Abs. 1981-2003/Jun
         (c) 2003 Info. Today Inc.
File  94:JICST-EPlus 1985-2003/Jul W3
         (c)2003 Japan Science and Tech Corp(JST)
File 603:Newspaper Abstracts 1984-1988
         (c)2001 ProQuest Info&Learning
File 483:Newspaper Abs Daily 1986-2003/Jul 25
         (c) 2003 ProQuest Info&Learning
File   6:NTIS 1964-2003/Jul W4
         (c) 2003 NTIS, Intl Cpyrght All Rights Res
File 144:Pascal 1973-2003/Jul W3
         (c) 2003 INIST/CNRS
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  34:SciSearch(R) Cited Ref Sci 1990-2003/Jul W3
         (c) 2003 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2003/Jun
         (c) 2003 The HW Wilson Co.
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
File 266:FEDRIP 2003/Jun
         Comp & dist by NTIS, Intl Copyright All Rights Res
File  95:TEME-Technology & Management 1989-2003/Jul W2
         (c) 2003 FIZ TECHNIK
File 438:Library Lit. & Info. Science 1984-2003/Jun
         (c) 2003 The HW Wilson Co
File 248:PIRA 1975-2003/Jul W4
         (c) 2003 Pira International

Set     Items   Description
S1      96476   REGISTER? ?
S2       7101   S1(5N)(ACCESS??? OR READ??? OR SCAN???? OR RETRIEV??? OR O-
             BTAIN??? OR GET???? OR POLL??? OR CHECK??? OR EXAMIN? OR ACQU-
             IR??? OR ACQUISITION OR TAP???? OR WRIT??? OR MANIPULAT? OR C-
             ONFIGUR? OR FETCH???)
S3     133654   (GRAPHIC? OR WINDOW?)(2W)INTERFACE? ? OR GUI OR GUIS OR BR-
             OWSER? ? OR GRAPHIC??(2W)(SCREEN? ? OR DISPLAY? ? OR PANE?? OR
              MONITOR? ? OR PROGRAM? OR APPLICATION? ? OR SOFTWARE)
S4     394219   CAD OR CAM OR CAE OR COMPUTER()(ASSISTED OR AIDED)()(DRAWI-
             NG OR DESIGN? OR MANUFACTUR??? OR ENGINEERING)
S5       5124   DEVICE? ?(5N)DRIVER? ?
S6        250   S2 AND S3:S4
S7        211   RD (unique items)
S8        188   S7 NOT PY=2001:2003
S9      10510   S1(5N)(DEVICE? ? OR PERIPHERAL? ? OR HARDWARE? ? OR MACHIN-
             E? ? OR UNIT? ? OR PROCESSOR? ? OR COMPUTER? ? OR PC? ? OR IN-
             STRUMENT? ? OR SETTOP OR BOX?? OR MODULE? ? OR EQUIPMENT? ? OR
              TERMINAL? ? OR CLIENT? ? OR WORKSTATION? ?)
S10       437   S1(5N)(WORK()STATION? ? OR PRINTER? ? OR COPIER? ? OR SCAN-
             NER? ? OR MONITOR? ?)
S11        46   S8 AND S9:S10
```

11/5/2 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04470026 E.I. No: EIP96083281471
Title: Register file and scheduling model for application specific processor synthesis
Author: Ercanli, E.; Papachristou, C.
Corporate Source: Case Western Reserve Univ, Cleveland, OH, USA
Conference Title: Proceedings of the 1996 33rd Annual Design Automation Conference
Conference Location: Las Vegas, NV, USA Conference Date: 19960603-19960607
Sponsor: IEEE
E.I. Conference No.: 45138
Source: Proceedings - Design Automation Conference 1996. IEEE, Piscataway, NJ, USA,96CH35932. p 35-40
Publication Year: 1996
CODEN: PDAWDJ ISSN: 0146-7123
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 9610W2
Abstract: In this paper, we outline general design steps of our synthesis tool to realize application specific co-processors such that for a given scientific application having intensive iterative computations especially with recurrences, a VLIW type of co-processor is synthesized and realized, and an accompanying parallel code is generated. We introduce a novel register file model, Shifting Register File (SRF), based on cyclic regularity of **register** file **accesses** ; and a simple method, Expansion Scheduling, for scheduling iterative computations, which is based on cyclic regularity of loops. We also present a variable-register file allocation method and show how simple logic units can be used to activate proper registers at run time through an example. (Author abstract) 8 Refs.
Descriptors: Parallel processing systems; Shift **registers** ; Iterative methods; Mathematical models; **Computer aided design**
Identifiers: Application specific **processors** ; Shift **register** file; Expansion scheduling
Classification Codes:
722.4 (Digital Computers & Systems); 721.3 (Computer Circuits); 921.6 (Numerical Methods); 723.5 (Computer Applications)
722 (Computer Hardware); 721 (Computer Circuits & Logic Elements); 921 (Applied Mathematics); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

11/5/3 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04274941 E.I. No: EIP95102902818
Title: New algorithm for sorting problem with reformed CAM
Author: Lu, Kuei-Ming; Tamaru, Keikichi
Corporate Source: Kyoto Univ, Kyoto, Jpn
Conference Title: Proceedings of the 1995 IEEE International Symposium on Circuits and Systems-ISCAS 95. Part 2 (of 3)
Conference Location: Seattle, WA, USA Conference Date: 19950430-19950503
Sponsor: IEEE
E.I. Conference No.: 43814
Source: Proceedings - IEEE International Symposium on Circuits and Systems v 2 1995. IEEE, Piscataway, NJ, USA,95CB35771. p 1045-1048
Publication Year: 1995
CODEN: PICSDI ISSN: 0271-4310
Language: English
Document Type: CA; (Conference Article) Treatment: A; (Applications); T ; (Theoretical)
Journal Announcement: 9512W3
Abstract: Nowadays, the addition of specific hardware to **CAD** or DA

application has been received by engineering community left bracket 1 right bracket . Specially, Content Addressable Memory (**CAM**) is in the limelight since its fast processing capability. In this paper, we propose a new algorithm and reformed **CAM** to deal with sorting problem that always takes the bulk execution time in some applications such as design-rule check, and they can reduce 80% retrieval times in comparison to the conventional one. (Author abstract) 9 Refs.

Descriptors: Algorithms; Sorting; Data storage equipment; Computer hardware; **Computer aided design** ; **Computer** simulation; Shift **registers** ; Computational complexity; Performance

Identifiers: Content addressable memory; Design rule **check** ; Data mask **register** ; Tag **register** ; Duplicate register; Garbage register; Plurality counter

Classification Codes:

723.1 (Computer Programming); 722.1 (Data Storage, Equipment & Techniques); 723.5 (Computer Applications); 721.3 (Computer Circuits); 721.1 (Computer Theory, Includes Formal Logic, Automata Theory, Switching Theory, Programming Theory)

723 (Computer Software); 722 (Computer Hardware); 721 (Computer Circuits & Logic Elements)

72 (COMPUTERS & DATA PROCESSING)

11/5/5 (Item 5 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

03930643 E.I. No: EIP94081372394

Title: Fragmented register architecture and test advisor for BIST

Author: Illman, R.J.; Traynor, D.J.

Corporate Source: ICL Corporate Systems

Conference Title: Proceedings of the European Design and Test Conference

Conference Location: Paris, Fr Conference Date: 19940228-19940303

Sponsor: European Design Automation Association; AEIA, Spain; Altium, an IBM Company; Bull SA, France; IEEE Computer Society; et al

E.I. Conference No.: 20750

Source: Proceedings of the European Design and Test Conference Proc Eur Des Test Conf 1994. Publ by IEEE, Computer Society Press, Los Alamitos, CA, USA. p 124-129

Publication Year: 1994

ISBN: 0-8186-5411-2

Language: English

Document Type: CA; (Conference Article) Treatment: T; (Theoretical)

Journal Announcement: 9410W2

Abstract: This paper describes two new developments in the implementation of quasi-exhaustive BIST. These are a new architecture, in which a conventional LFSR/MISR is broken down into three separate elements, and a **CAD** ?test advisor' which provides a fast check of BIST DFT rules and informs the chip designer how to **configure** the **registers** and LFSRs within a design. These two new developments are closely interdependent and give a major increase in DFT productivity when implementing BIST. (Author abstract) 6 Refs.

Descriptors: Integrated circuit testing; Shift **registers** ; Microprocessor chips; Fast Fourier transforms; **Computer** architecture; Error detection; Probability; Computer circuits

Identifiers: Fragmented register architecture; Test advisor; Built in self test

Classification Codes:

713.5 (Other Electronic Circuits); 721.3 (Computer Circuits); 921.3 (Mathematical Transformations); 722.4 (Digital Computers & Systems); 921.6 (Numerical Methods); 922.1 (Probability Theory)

713 (Electronic Circuits); 721 (Computer Circuits & Logic Elements); 921 (Applied Mathematics); 722 (Computer Hardware); 922 (Statistical Methods)

71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

11/5/6 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03450734 E.I. Monthly No: EI9207085645
Title: Embedded PCs boost evolution of VXI architecture.
Author: Anon
Source: EE: Evaluation Engineering v 31 n 2 Feb 1992 p 46-47
Publication Year: 1992
CODEN: EVENAE ISSN: 0149-0370
Language: English
Document Type: JA; (Journal Article) Treatment: A; (Applications)
Journal Announcement: 9207
Abstract: The PC offers many advantages as an instrumentation system controller. With more than 50 million installed, the PC has achieved a high level of familiarity and pervasiveness in the industry today. Software development tools such as compilers and debuggers, human interface and **graphical display** packages, and sophisticated instrument control and data acquisition packages have been on the market for the PC for many years. Embedding the PC into the VXI chassis provides three additional advantages consistent with the primary benefits of the VXIbus architecture: performance, size and ruggedness. Direct access to the VXIbus backplane allows data to be transferred between the controller and the VXI instruments in the system at VME speeds of several megabytes per second. Software running on the embedded PC also can directly **access** memory residing on **register** -based **instruments** or VME **modules** as though it were local PC memory, further improving overall system throughput.
Descriptors: *COMPUTER ARCHITECTURE--*Performance; COMPUTERS, PERSONAL; ELECTRIC MEASURING INSTRUMENTS; COMPUTER HARDWARE; COMPUTER SOFTWARE
Identifiers: EMBEDDED PC; VXI ARCHITECTURE
Classification Codes:
722 (Computer Hardware); 723 (Computer Software); 942 (Electrical & Electronic Measuring Instruments); 941 (Acoustical & Optical Measuring Instruments); 943 (Mechanical & Miscellaneous Measuring Instruments); 944 (Moisture, Pressure & Temperature, & Radiation Measuring Instruments)
72 (COMPUTERS & DATA PROCESSING); 94 (INSTRUMENTS & MEASUREMENT)

11/5/9 (Item 9 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02583505 E.I. Monthly No: EI8806052262
Title: TRIPLE-PORT DRAM FUELS GRAPHIC DISPLAYS .
Author: Bursky, Dave
Source: Electronic Design v 35 n 10 Apr 30 1987 p 53-54
Publication Year: 1987
CODEN: ELODAW ISSN: 0013-4872
Language: English
Document Type: JA; (Journal Article) Treatment: A; (Applications)
Journal Announcement: 8806
Abstract: The mu PD42232C/LA video RAM, a CMOS dynamic RAM with three **access** ports and multiple programmable **registers** , is described. The **device** contains an array of dynamic RAM cells organized as 32 kwords-by-8 bits and an asynchronous 128 word-by-8-bit serial read/write buffer. Depending on the version, the random-access port will have an access time of either 100, 120, or 150 ns while the serial-access ports will handle data at 30, 40, or 60 ns per bit, respectively. The central-memory array can transfer data in any of three ways to the display - through an 8-bit common I/O port; by means of a serial pixel-access port; or through a serial 128-word-by-8-bit I/O buffer. The system interface on the chip's host side is much like that of most other dynamic RAMs.
Descriptors: *DATA STORAGE, DIGITAL--*Random Access; DISPLAY DEVICES--Components; COMPUTER PERIPHERAL EQUIPMENT--Graphics; SEMICONDUCTOR DEVICES, MOS--Applications
Identifiers: TRIPLE-PORT DRAM; **GRAPHIC DISPLAYS** ; CMOS DYNAMIC RAM
Classification Codes:
721 (Computer Circuits & Logic Elements); 722 (Computer Hardware); 741

(Optics & Optical Devices); 714 (Electronic Components)
72 (COMPUTERS & DATA PROCESSING); 74 (OPTICAL TECHNOLOGY); 71 (ELECTRONICS & COMMUNICATIONS)

11/5/11 (Item 11 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01751401 E.I. Monthly No: EI8505037447 E.I. Yearly No: EI85057711
Title: MEANS FOR EXECUTING REGISTER -TO- REGISTER **INSTRUCTIONS IN A** COMPUTER **WITH A SINGLE-PORT LOCAL STORE.**
Author: Olnowich, H.; Vandling, G.
Source: IBM Technical Disclosure Bulletin v 27 n 8 Jan 1985 p 4646
Publication Year: 1985
CODEN: IBMTAA ISSN: 0018-8689 ISBN: 0-87079-126-5
Language: ENGLISH
Document Type: JA; (Journal Article) Treatment: A; (Applications)
Journal Announcement: 8505
Abstract: In general-purpose **computers** with storage operand prefetch, **Register** -to-Register (RR) instructions inherently execute in approximately the same amount of time as their corresponding Storage-to-Register (RX) instructions. In a pipelined design which has a two-port local store, the cycle used for effective addressing for an RX instruction is unused for a corresponding RR instruction. When an Arithmetic and Logic Unit (ALU) with a single-port local store is used, the storage operand is prefetched and the first operand can be fetched from the local store, allowing RX instruction execution with no problem. A method to **fetch** a second **register** operand, without requiring additional time, is to prefetch the second register operand in advance during the time slot corresponding to the Effective Address (EA) slot for an RX instruction. Thus, the complexity (area) of local store is significantly reduced in an LSI design.
Descriptors: INTEGRATED CIRCUITS, LSI--* **Computer Aided Design** ; DATA STORAGE, DIGITAL
Identifiers: REGISTER-TO-REGISTER INSTRUCTIONS; SINGLE-PORT LOCAL STORE
Classification Codes:
713 (Electronic Circuits); 714 (Electronic Components); 723 (Computer Software); 721 (Computer Circuits & Logic Elements)
71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING)

11/5/12 (Item 12 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01188812 E.I. Monthly No: EI8206051246 E.I. Yearly No: EI82057927
Title: AUTOMATED SYNTHESIS OF DIGITAL HARDWARE.
Author: Hafer, Louis J.; Parker, Alice C.
Corporate Source: Simon Fraser Univ, Vancouver, BC, Can
Source: IEEE Transactions on Computers v C-31 n 2 Feb 1982 p 93-109
Publication Year: 1982
CODEN: ITCOB4 ISSN: 0018-9340
Language: ENGLISH
Journal Announcement: 8206
Abstract: A description is given of a portion of the Carnegie-Mellon University Design Automation (CMU-DA) research. This part involves the design and construction of a data-memory allocator, consisting of a set of algorithms and data structures which synthesize **hardware** at the **register** -transfer level from a behavioral description **written** in ISP. The allocator selects **registers** and data operators and interconnects them with data paths to form a data part capable of implementing the data operations specified in the behavior. Results indicate that the allocator's performance compares favorably with a human designer when designing an elevator controller and a reduced PDP-8/E. Although optimal designs cannot be guaranteed, upper bounds for the number of components used can be derived from the ISP description. 34 refs.
Descriptors: LOGIC DESIGN; **COMPUTER AIDED DESIGN**
Classification Codes:

721 (Computer Circuits & Logic Elements); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING)

11/5/14 (Item 2 from file: 202)
DIALOG(R)File 202:Info. Sci. & Tech. Abs.

2702435
Method for accessing microprocessor and microinstruction control type microprocessor including pointer register.
Author(s): Nagata, M
Patent Number(s): US 5117487
Publication Date: May 26, 1992
Language: English
Document Type: Patent
Record Type: Abstract
Journal Announcement: 2700

In a microprocessor, a microinstruction is used to control the microprocessor. The microprocessor includes: a decoder for decoding the STC instruction to obtain a decoded instruction and address data, the address data designating an address of a control space allocated to a plurality of registers in a general-purpose register group; an address register for temporarily storing the address data derived from the decoder; a microinstruction storage unit for previously storing a plurality of microinstructions and for outputting the microinstruction one by one in response to the decoded instruction; a microinstruction register for producing a control signal in response to the read microinstruction; a calculation unit for calculating the address data stored in the address **register** means to **obtain** bit information of the address data for designating a specific register in response to the bit information derived from the calculation **unit** , while the general-purpose **register** group; and, a pointer register for temporarily storing the bit information to **access** the specific **register** in response to the bit information derived from the calculation **unit** , while the general-purpose **register** group is instructed in response to the control signal.

Descriptors: Access methods; Decoding; Microprocessors; Patents
Classification Codes and Description: 5.05 (Hardware); 5.08 (**Graphics** and **Displays**)
Main Heading: Information Processing and Control

11/5/15 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5834266 INSPEC Abstract Number: B9803-1265B-062, C9803-5210B-039
Title: Formalizing the logic design of register components in discrete systems
Author(s): Mishchenko, A.A.; Mishchenko, A.T.
Journal: Kibernetika i Sistemnyi Analiz vol.33, no.2 p.32-44
Publisher: Plenum,
Publication Date: March-April 1997 Country of Publication: Ukraine
CODEN: KSANE9
Material Identity Number: P784-98001
Translated in: Cybernetics and Systems Analysis vol.33, no.2 p.177-85
Publication Date: March-April 1997 Country of Publication: USA
CODEN: CYASEC ISSN: 1060-0396
SICI of Translation: 1060-0396(199703/04)33:2L.177:FLDR;1-U
U.S. Copyright Clearance Center Code: 1060-0396/97/3302-0177$18.00
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: Discrete hardware design involves at a certain stage the logic design of three types of components: functional components (combinational logic networks), operational components (registers), and control components (automata). Control automata design has been developed in considerable

detail, while formal (and thus **computer** -aided) **register** design still involves difficulties, despite its apparent simplicity. In practice, register design uses various flip flops as storage elements, and each type of flip flop can be implemented by dozens of different logic circuits with different reliability characteristics and optimization options. Moreover, **writing** data to a **register** may involve more than ten different register operations. The designer thus has to choose the hardware solution from a large number of options, allowing for the time characteristics of the input signals, as well as requirements for speed, cost-efficiency, reliability, etc. The article proposes a solution to this problem through the development of a formal register design procedure originally described in (Glushkov, 1987). The designer, using his experience and intuition, allows for a variety of circumstances and constraints, selects some register design, and describes its operating algorithm in an accessible language. The register circuit is then constructed on the basis of this algorithm. The simplicity of the procedure enables the designer to foresee the outcome of the **computer - aided design** procedure. (4 Refs)

Subfile: B C

Descriptors: automata theory; circuit optimisation; flip-flops; logic **CAD**

Identifiers: logic design; register components; discrete systems; hardware design; functional components; combinational logic networks; operational components; flip flops; control components; control automata design; **computer** -aided **register** design; logic circuits; reliability; optimization

Class Codes: B1265B (Logic circuits); B1130B (Computer-aided circuit analysis and design); C5210B (Computer-aided logic design); C5120 (Logic and switching circuits)

11/5/18 (Item 4 from file: 2)

DIALOG(R)File 2:INSPEC

5572417 INSPEC Abstract Number: B9706-1265-015, C9706-5210B-068

Title: A graph-theoretic approach for register file based synthesis

Author(s): Ravikumar, C.P.; Aggarwal, R.; Sharma, C.

Author Affiliation: Dept. of Electr. Eng., Indian Inst. of Technol., New Delhi, India

Conference Title: Proceedings. Tenth International Conference on VLSI Design (Cat. No.97TB100095) p.118-23

Publisher: IEEE Comput. Soc. Press, Los Alamitos, CA, USA

Publication Date: 1997 Country of Publication: USA xxxvii+566 pp.

ISBN: 0 8186 7755 4 Material Identity Number: XX97-00085

U.S. Copyright Clearance Center Code: 0 8186 7755 4/96/$05.00

Conference Title: Proceedings Tenth International Conference on VLSI Design

Conference Sponsor: VLSI Soc. India; Dept. Electron., Gov. India; IEEE; IEEE Comput. Soc. Tech. Committee on Design Autom.; IEEE Comput. Soc. Tech. Committee on VLSI; IEEE Circuits & Syst. Soc.; ACM SIGDA

Conference Date: 4-7 Jan. 1997 Conference Location: Hyderabad, India

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P); Theoretical (T)

Abstract: With the increasing use of register files as storage elements in integrated circuits, the problem of assigning data variables to ports of register files has assumed significance. The assignment involves simultaneous optimization of several cost functions, namely, number of **register** files, number of **registers** and **access** ports per **register** file, and the interconnect both internal and external to memories. In this paper, we refer to multiplexers, busses, and tristate switches when we refer to interconnect. The objective of this paper is to describe graph-theoretic optimization algorithms for the assignment problem. The allocation system described in this paper (SOUPS) accepts a scheduled data flow graph as input and performs (i) assignment of variables to a minimal number of resisters, (ii) assignments of registers to a minimal number of register files, (iii) assignment of registers to ports of the register files using minimal interconnect within the register files, and (iv)

assignment of ports of the **register** files to terminals of functional **modules** using minimal interconnect outside the **register** files. We describe experimental results on several benchmark problems. (9 Refs)

Subfile: B C

Descriptors: circuit layout **CAD** ; circuit optimisation; data flow graphs ; integrated circuit interconnections; integrated circuit layout; logic **CAD**

Identifiers: register file based synthesis; graph-theoretic approach; storage elements; integrated circuits; data variables; simultaneous optimization using parallel synthesis; cost functions; access ports; interconnect; multiplexers; busses; tristate switches; graph-theoretic optimization algorithms; SOUPS; scheduled data flow graph; variable assignment; functional module terminals; benchmark problems

Class Codes: B1265 (Digital electronics); B1130B (Computer-aided circuit analysis and design); B2570 (Semiconductor integrated circuits); B0250 (Combinatorial mathematics); C5210B (Computer-aided logic design); C1160 (Combinatorial mathematics); C7410D (Electronic engineering computing)

11/5/19 (Item 5 from file: 2)

DIALOG(R)File 2:INSPEC

5217832 INSPEC Abstract Number: B9605-1265B-015, C9605-7410D-058

Title: Design for testability using register **-transfer level partial** scan **selection**

Author(s): Motohara, A.; Takeoka, S.; Hosokawa, T.; Ohta, M.; Takai, Y.; Matsumoto, M.; Muraoka, M.

Author Affiliation: Semicond. Res. Center, Matsushita Electr. Ind. Co. Ltd., Moriguchi, Japan

Conference Title: Proceedings of the ASP-DAC`95/CHDL`95/VLSI`95. Asia and South Pacific Design Automation Conference. IFIP International Conference on Computer Hardware Description Languages and their Applications. IFIP Interntional Conference on Very Large Scale Integration (IEEE Cat. No.95TH8102) p.209-15

Publisher: Nihon Gakkai Jimu Senta, Tokyo, Japan

Publication Date: 1995 Country of Publication: Japan xxxii+860 pp.

ISBN: 4 930813 67 0 Material Identity Number: XX94-02583

Conference Title: Proceedings of ASP-DAC`95/CHDL`95/VLSI`95 with EDA Technofair

Conference Sponsor: IFIP WG 10.5 (Former 10.2 & 10.5); IEICE; IPSJ (Inf. Process. Soc. Japan); ACM SIGDA; IEEE Circuits & Syst. Soc.; IEEE Comput. Soc

Conference Date: 29 Aug.-1 Sept. 1995 Conference Location: Chiba, Japan

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: An approach to top down design for testability using **register** -transfer level (RTL) partial **scan** selection is described. We propose a scan selection technique based on testability analysis for RTL design including data path circuits and control circuits such as state **machines** . **Registers** and state **machines** which make gate level ATPG difficult are identified by the scan selection technique based on RTL testability analysis effectively. Experimental results for actual circuits are also presented. (19 Refs)

Subfile: B C

Descriptors: design for testability; finite state machines; integrated circuit design; integrated circuit testing; logic **CAD** ; logic gates; logic testing; VLSI

Identifiers: design for testability; register-transfer level design; partial scan selection; top down design; testability analysis; RTL design; data path circuits; control circuits; state machines; registers; gate level ATPG; experimental results; VLSI design; **CAD**

Class Codes: B1265B (Logic circuits); B1130B (Computer-aided circuit analysis and design); B2570 (Semiconductor integrated circuits); C7410D (Electronic engineering computing); C5210B (Computer-aided logic design)

11/5/22 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

4976221 INSPEC Abstract Number: C9508-0310H-001
Title: Choosing the right software for data acquisition
Author(s): House, R.
Author Affiliation: Nat. Instrum. Corp., Austin, TX, USA
Journal: IEEE Spectrum vol.32, no.5 p.24-6, 28-32, 34-9
Publication Date: May 1995 Country of Publication: USA
CODEN: IEESAM ISSN: 0018-9235
U.S. Copyright Clearance Center Code: 0018-9235/95/$4.00
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Product Review (R)
Abstract: The subject of this report is any software that interfaces either with plug-in data acquisition (DAQ) boards or with external DAQ boxes. Embedded in it is the binary code needed to **configure** the **registers** of the **box** or board for analog, digital, and timing input/output. The software controls the gain per channel, sampling rate, sampling order, digital levels, and counter and timer control. It also controls the transfer of data to and from the board or box by polling, interrupts, or direct memory access. Multitasking and/or **graphical programming** and/or virtual instrumentation enhance the packages for use in process monitoring and control, test, measurement, and more. The author describes the main features of DAQ software and gives advice on how to choose the best package for a particular application. A table is given listing over 50 software packages. (5 Refs)
Subfile: C
Descriptors: data acquisition; software packages; software reviews; software selection
Identifiers: data acquisition software; plug-in data acquisition boards; external DAQ boxes; binary code; gain per channel; sampling rate; sampling order; digital levels; timer control; counter control; direct memory access ; multitasking; **graphical programming** ; virtual instrumentation; process monitoring
Class Codes: C0310H (Equipment and software evaluation methods); C7410H (Computerised instrumentation); C5520 (Data acquisition equipment and techniques)

11/5/23 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

4514668 INSPEC Abstract Number: B9312-1130B-010, C9312-4230D-001
Title: Formal verification of sequential hardware: a tutorial
Author(s): McFarland, M.C.
Author Affiliation: Dept. of Comput. Sci., Boston Coll., Chestnut Hill, MA, USA
Journal: IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems vol.12, no.5 p.633-54
Publication Date: May 1993 Country of Publication: USA
CODEN: ITCSDI ISSN: 0278-0070
U.S. Copyright Clearance Center Code: 0278-0070/93/$03.00
Language: English Document Type: Journal Paper (JP)
Treatment: Bibliography (B); Theoretical (T)
Abstract: Various formal verification techniques and how they can be applied to sequential **hardware** , especially at the **register** -transfer level, are **examined** . The basic elements of a verification system, as illustrated on the relatively simple problem of verifying combinational circuits, are presented. The more complex problems involved in analyzing sequential systems and the techniques that have been developed to solve them are then considered. Throughout, the focus is on those techniques whose utility has been demonstrated on real systems, including higher order logic, temporal logic, predicate transformers, state-machine models, and

model checkers. (76 refs)
Subfile: B C
Descriptors: logic **CAD** ; sequential circuits; sequential machines; sequential switching; switching theory
Identifiers: sequential hardware; formal verification techniques; register-transfer level; higher order logic; temporal logic; predicate transformers; state-machine models; model checkers
Class Codes: B1130B (Computer-aided circuit analysis and design); B1265B (Logic circuits); C4230D (Sequential switching theory); C7410D (Electronic engineering); C5210B (Computer-aided logic design)

11/5/24 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC

04391350 INSPEC Abstract Number: B9306-1130B-006, C9306-6115-010
Title: System prototyping with ALMA
Author(s): Brunel, J.Y.; Auge, I.; Redon, X.; Tychon, P.
Author Affiliation: Lab. d'Electron. Philips, Limeil-brevannes, France
Conference Title: Second International Workshop on Rapid System Prototyping. Shortening the Path from Specification to Prototype (Cat. No.92TH0454-9) p.103-9
Editor(s): Kanapoulos, N.
Publisher: IEEE Comput. Soc. Press, Los Alamitos, CA, USA
Publication Date: 1992 Country of Publication: USA viii+201 pp.
ISBN: 0 8186 3040 X
U.S. Copyright Clearance Center Code: 0 8186 3040 X/92$3.00
Conference Sponsor: IEEE; ACM
Conference Date: 11-13 June 1991 Conference Location: Research Triangle Park, NC, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: ALMA presents itself like a shell over a **CAD** framework. It mainly aims at portable description (independent on **CAD** framework); rapid system modelling (using a powerful temporal and functional simulator), and quick realization (using a sequential language **manipulating hardware** resources like **registers** , ALUs). The ALMA strongest point is its practical side. It offers entry points within the system at two different levels. The first level gives the possibility to install new resources in the input language. Except on installation phases for these new resources, this level is a portable entry. The second level is to directly bring into the simulator manually designed blocks by describing their models. Such a feature is of course not portable. Finally, ALMA relations to **CAD** frameworks look a little bit like Unix relations to computers. ALMA is a general purpose kernel, but this kernel is open, and the user can focus itself onto a specific application domain. (7 Refs)
Subfile: B C
Descriptors: circuit analysis computing; software prototyping; software tools; specification languages; virtual machines
Identifiers: **CAD** framework; portable description; rapid system modelling; functional simulator; sequential language manipulating hardware resources; ALMA; new resources; input language; portable entry; general purpose kernel; application domain
Class Codes: B1130B (Computer-aided circuit analysis and design); C6115 (Programming support); C6110B (Software engineering techniques); C7430 (Computer engineering); C6140D (High level languages); C7410D (Electronic engineering)

11/5/27 (Item 13 from file: 2)
DIALOG(R)File 2:INSPEC

03471807 INSPEC Abstract Number: B89060765, C89061669
Title: Testability strategy for registers and memories in a multi-processor architecture
Author(s): van Sas, J.; Catthoor, F.; Inze, L.; De Man, H.

Author Affiliation: IMEC Lab., Leuven, Belgium
Conference Title: Proceedings of the 1st European Test Conference (IEEE Cat. No.89CH2696-3) p.294-303
Publisher: IEEE Comput. Soc. Press, Washington, DC, USA
Publication Date: 1989 Country of Publication: USA xiv+417 pp.
ISBN: 0 8186 1937 6
U.S. Copyright Clearance Center Code: CH2696-3/89/0000-0294$01.00
Conference Sponsor: IEEE
Conference Date: 12-14 April 1989 Conference Location: Paris, France
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: A testability strategy is presented for registers and memories embedded in multiprocessor chips designed with the Cathedral-II silicon compilation environment. The implementation requires the design of a **scan register** that is able to maintain a value at its output while scanning a vector into the scan chain. A test algorithm for the register file, based on the concept of C-testability, is derived. The fault model covers both stuck-at and most of the transistor stuck-open and stuck-close cases. In addition, large embedded memories are important in processor systems. A test strategy with very high fault coverage is implemented with a self-test approach. (19 Refs)
Subfile: B C
Descriptors: circuit **CAD** ; computer architecture; computer equipment testing; fault location; integrated memory circuits; logic testing; multiprocessing systems; shift registers
Identifiers: computer equipment testing; multi-processor architecture; testability strategy; multiprocessor chips; Cathedral-II silicon compilation environment; **scan register** ; scan chain; test algorithm; register file; C-testability; fault model; stuck-at; stuck-open; stuck-close; embedded memories; self-test
Class Codes: B1265B (Logic circuits); B1265D (Memory circuits); C5320G (Semiconductor storage); C5470 (Performance evaluation and testing); C5210 (Logic design methods); C5440 (Multiprocessor systems and techniques); C5220 (Computer architecture); C7410D (Electronic engineering); C7430 (Computer engineering)

11/5/36 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01004986 JICST ACCESSION NUMBER: 90A0408301 FILE SEGMENT: JICST-E
Function and logic design system.
SEKINE MASATOSHI (1); NISHIO SEIICHI (1)
(1) Toshiba Corp.
Toshiba Rebyu(Toshiba Review), 1990, VOL.45,NO.4, PAGE.360-363, FIG.5, TBL.1, REF.4
JOURNAL NUMBER: F0360AAK ISSN NO: 0372-0462 CODEN: TORBA
UNIVERSAL DECIMAL CLASSIFICATION: 621.37:681.325.6
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: A functional design system has been developed to design functionalities of logic circuits by describing them as data flows and operations with execution conditions. The designer **writes** functional models at the **register** transfer level using either the **hardware** design language H2DL, developed by Toshiba, or a functional block diagram. A mixed-level simulator is employed to verify the correctness of the functional design, and a logic synthesizer translates the completed functional models into logic circuits with logic design rules. Functional blocks are translated directly to the optimum logic circuits, and the local transformation algorithm generates control logic circuits. This system has been in practical use since 1985, and has achieved considerable reductions in design time. (author abst.)
DESCRIPTORS: logical design; **CAD** ; logic circuit; circuit design; VLSI; logic element; logic simulation; system design
BROADER DESCRIPTORS: design; computer application; utilization; circuit;

LSI; integrated circuit; micro circuit; functional device; computer simulation; simulation
CLASSIFICATION CODE(S): NC05070B

11/5/46 (Item 5 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00627283 I92091152928
DSS: a distributed high-level synthesis system
(DSS-Algorithmen- und alternativer VLSI-Entwurf)
Roy, J; Kumar, N; Dutta, R; Vemuri, R
Cincinnati Univ., OH, USA
IEEE Design and Test of Computers, v9, n2, pp18-32, 1992
Document type: journal article Language: English
Record type: Abstract
ISSN: 0740-7475

ABSTRACT:
DSS, a large-scale ongoing exercise in developing parallel algorithms for high-level synthesis and implementing them in an integrated distributed system to evaluate their individual and collective effectiveness, is discussed. Embedded in a very-high-speed integrated circuit hardware description language (VHDL) centered design environment, DSS consists of a collection of parallel algorithms executing on a multiple input, multiple data (MIMD) multiprocessor machine. The system uses coarse-grained parallelism to explore and evaluate many alternative VLSI designs efficiently. DSSs internal organization and its scheduling, register optimization, interconnection formation, and controller generation techniques are described. Results illustrating DSS performance with respect to design quality, and the efficiency of the DSS algorithms in a multiprocessor environment are presented.

DESCRIPTORS: DISTRIBUTED COMPUTING; PARALLEL ALGORITHMS; DESCRIPTION LANGUAGES; GRAND SCALE INTEGRATION; IMPLEMENTATION; CIRCUIT **CAD** ; **ACCESS** CONTROL; MULTIPROCESSING SYSTEMS; **REGISTER** --MEMORY; VERY HIGH SPEED INTEGRATED CIRCUITS; MULTIPLE ACCESS; DATA INPUT OUTPUT; PERFORMANCE EVALUATION; CIRCUIT ANALYSIS COMPUTING; PERFORMANCE
IDENTIFIERS: VHDL; MIMD; DISTRIBUTED HIGH LEVEL SYNTHESIS SYSTEM; INTEGRATED DISTRIBUTED SYSTEM; MULTIPROCESSOR **MACHINE** ; COARSE GRAINED PARALLELISM; VLSI DESIGNS; **REGISTER** OPTIMIZATION; INTERCONNECTION FORMATION; CONTROLLER GENERATION; DESIGN QUALITY; verteilte Synthese; Multiprozessor
?

02425435 SUPPLIER NUMBER: 63919472 (THIS IS THE FULL TEXT)

Regent register-creation tool expands to include software designers. (Product Announcement)

Goering, Richard

Electronic Engineering Times, 58
August 7, 2000
DOCUMENT TYPE: Product Announcement ISSN: 0192-1541 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 413 LINE COUNT: 00037

TEXT:

MARLBORO, MASS. - Innoveda Inc. has expanded Regent, a spreadsheet-like register specification tool, to serve both hardware and software designers. Regent was introduced by Summit Design Inc. before that company merged with Viewlogic Systems Inc. to become Innoveda. The new Regent 2.0 is Innoveda's first release of the tool.

Regent provides a **graphical** user **interface** that lets **hardware** and system designers describe system **registers** . Users enter information like **register** names, addresses and **access** attributes. Users also specify the bus interface. The tool supports standard buses like ARM Ltd.'s Amba and IBM Corp.'s DCR and permits users to define bus interfaces with VHDL or Verilog.

First shipped in late 1999, the initial product generated synthesizable HDL code for hardware designers. The enhanced Regent 2.0 adds generation of C language header files for software developers. These header files capture the register table structure and generate read/write macros for each field based on its specific size, mapping and access rights. The header file is updated with every change in the register table.

The result is a single register image serving both hardware and software designers, said Rami Rachamim, Innoveda director of system-level design product marketing.

"The header files save a significant amount of time and avoid a significant number of iterations between the two groups," Rachamim said. "These can be very large files, and they're hard to maintain. A large system can end up with 40,000 or 50,000 registers."

A second enhancement in version 2.0 is a graphical register table that shows how fields are mapped to logical registers. With this feature, said Rachamim, users can "drag and drop" the contents of various fields between memory-mapped registers, while tracking address changes.

The ability of the tool to read and generate Excel tables, including lists of registers, fields, signals and ports, is a third enhancement.

Even though Regent started out with a spreadsheet-like interface, the original version didn't have the ability to read and write Excel files, Rachamim said. But users had a lot of legacy data in Excel spreadsheets they wanted to move over into Regent.

Regent 2.0 is available now as a standalone tool or as a licensed option with Innoveda's Visual HDL product. Regent 2.0 runs on Unix and Windows platforms, priced starting at $15,000. Additional information is at www.innoveda.com.

http://www.eetimes.com/

COMPANY NAMES: Innoveda Inc.--Product introduction
GEOGRAPHIC CODES/NAMES: 1USA United States
DESCRIPTORS: CAE software; Software product introduction
EVENT CODES/NAMES: 336 Product introduction
PRODUCT/INDUSTRY NAMES: 7372434 (Electrical Engineering Software)
SIC CODES: 7372 Prepackaged software
NAICS CODES: 51121 Software Publishers
TRADE NAMES: Innoveda Regent 2.0 (CAE software)--Product introduction
FILE SEGMENT: CD File 275

09812303 SUPPLIER NUMBER: 19921612 (THIS IS THE FULL TEXT)

SuperTAP(TM) 860T and SuperTAP 860SAR Emulators Now Available From Applied Microsystems

PR Newswire, p1027SFM084
Oct 27, 1997
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 681 LINE COUNT: 00063

TEXT:

REDMOND, Wash., Oct. 27 /PRNewswire/ -- Applied Microsystems Corporation (Nasdaq: APMC) today announced support for Motorola's MPC860T and MPC860SAR microprocessors. The SuperTAP(TM) 860T and 860SAR emulators are the latest in a continuing series of SuperTAPs, Applied's full-featured, small form-factor emulator. Without removing any key features, Applied has shrunk full-scale emulation to roughly one-tenth the size and weight of typical chassis-based emulators. SuperTAPs cost one third to one half that of competitive products.

The MPC860T is a highly integrated microprocessor used for networking applications such as remote access routers and remote access servers. It is also used in telecommunications applications such as switch controllers and PBX controllers. Its single, fast Ethernet connection makes it a cost-effective solution for internetworking applications.

The MPC860SAR includes Segmentation and Reassembly (SAR) functionality and is designed specifically for xDSL devices, telecommunications equipment, multimedia devices and other internetworking applications that require ATM (Asynchronous Transfer Mode).

Features of SuperTAP 860T and SuperTAP 860SAR Emulators

The new SuperTAP 860T and SuperTAP 860SAR provide, crash-proof, full-scale emulation for all speed grades and variants of the MPC860T and MPC860SAR respectively. SuperTAP 860T and 860SAR emulators provide Ethernet communications support for the IEEE TCP/IP frame format specification. Additional bus support features include 4-state, real-time nested event detection for a single thread event on each bus cycle and real-time trace.

To compress development schedules, SuperTAP 860T and 860SAR include special features for debugging, including a 128K real-time trace system, a trace disassembler, a CPU register browser, and a real-time complex event detection system. SuperTAP offers flash memory download support for 3v, 5v and 12v devices in 8-, 16- and 32-bit bus widths.

The trace and disassembler system allows the user to view software execution as well as to trace and debug code in real-time as it runs in the processor's instruction cache. Software trace and debug can also occur in external memory. Overlay memory is available with 8 MB configurations with one wait-state at 50MHz.

With the on-line visual **register browser** too), engineers can quickly **configure** and save the content of the **processor** 's integrated CPM **registers** , The event system enables real-time detection of events in the target system and high-speed programmability to support detection of events at both the bus cycle and software logic levels.

An integrated source-level debugger interface is provided by MWX-ICE, which supports Sun4, Windows/95, Windows/NT and HP9000 host platforms. MWX-ICE is integrated with ISI's pSOS and Wind River's VxWorks kernels using Applied's RTOS-Link O/S visibility tool. Integrated C/C++ support for PowerPC compilers generating ELF/Dwarf format include software from Diab Data, Green Hills, GNU, Metaware and MRI.

Price and Availability for SuperTAP 860T/860SAR

The SuperTAP 860T and SuperTAP 860SAR are available, today with immediate delivery. A typical system price for 40MHz support, 64K trace, IMB overlay memory, 24-bit time stamp and an Ethernet communications interface for a PC host is priced under U.S. $20,000.

About Applied Microsystems

The leader in hardware-enhanced embedded software design, debug and test solutions, Applied Microsystems helps engineers develop products faster, more reliably and at a lower cost-per-engineer. Applied's tools include: innovative coverification tools; in-circuit emulators, from

low-cost models designed especially for software engineers, to powerful full-scale models for both software and hardware development; and category-defining embedded software verification tools.

11/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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02425435 SUPPLIER NUMBER: 63919472 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Regent register-creation tool expands to include software designers. (Product Announcement)
Goering, Richard
Electronic Engineering Times, 58
August 7, 2000
DOCUMENT TYPE: Product Announcement ISSN: 0192-1541 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 413 LINE COUNT: 00037

Regent provides a **graphical** user **interface** that lets **hardware** and system designers describe system **registers** . Users enter information like **register** names, addresses and **access** attributes. Users also specify the bus interface. The tool supports standard buses like ARM Ltd...

11/3,K/2 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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02158143 SUPPLIER NUMBER: 20466349 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Ways to Broaden the Breadth of Browsers; Kits for Communicator, IE let companies adapt tools, PC Week Labs finds. (Product Announcement)
Rapoza, Jim
PC Week, v15, n14, p38(1)
April 6, 1998
DOCUMENT TYPE: Product Announcement ISSN: 0740-1604 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 552 LINE COUNT: 00048

... s Client Customization Kit simply changes a few configuration files.
For more information or to **register** for Netscape's **Client** Customization Kit, go to home.netscape.com/comprod/netscape...

...programs/ **browser** _...

...product.html. To **get** more information or to **register** for Microsoft's IEAK, go to ieak.microsoft.com.
Netscape's Client Customization Kit creates

11/3,K/3 (Item 3 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2003 The Gale Group. All rts. reserv.

01713338 SUPPLIER NUMBER: 16434120 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Image processing: past and present. (DataCube Inc VP Scott Roth) (Interview)
Lasers & Optronics, v13, n7, p29(2)
July, 1994
DOCUMENT TYPE: Interview ISSN: 0892-9947 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2445 LINE COUNT: 00184

... S.R.: On the software side, years ago we were working in assembly language and **writing** directly to **hardware** **registers** . That evolved to C and C libraries because the process became too tedious, too complicated for direct work at the register level. That's now evolving further to **graphical** user **interfaces** (**GUIs**).
L&O: And sensor evolution?
S.R.: The primary sensor technology of ten or fifteen...

11/3,K/4 (Item 4 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01648277 SUPPLIER NUMBER: 16251628
NetPro's StreetWise eases VINES management. (Software Review) (NetPro Computing's StreetWise 1.1 Windows management utility) (Evaluation)
Martin, Greg
Network Computing, v5, n9, p122(2)
August 1, 1994
DOCUMENT TYPE: Evaluation ISSN: 1046-4468 LANGUAGE: ENGLISH
RECORD TYPE: ABSTRACT

...ABSTRACT: an Alert Management Service to monitor server events and conditions, it lacks any tools to **configure** it. StreetWise can **register devices** with the service and set thresholds through a **Windows interface** .

11/3,K/5 (Item 5 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01625057 SUPPLIER NUMBER: 14445442 (USE FORMAT 7 OR 9 FOR FULL TEXT)
ICE for Pentium runs at full 66-MHz. (New Product Developments) (Microtek International Inc. Development Systems Division's in-circuit Pentium emulator) (Product Announcement)
Williams, Tom
Computer Design, v32, n9, p116(1)
Sept, 1993
DOCUMENT TYPE: Product Announcement ISSN: 0010-4566 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 536 LINE COUNT: 00042

... 33-MHz PC host computer running Microsoft Windows 3.1. It uses its own custom **Windows** -based user **interface** that connects with all the emulator features and provides for C source debugging with interleaved display of assembly code. Other windows are dedicated to memory and **register manipulation** , call-stack, variable watch, **module** , inspector and trace. The memory windows can automatically locate the descriptor tables and let the...

11/3,K/6 (Item 6 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01454459 SUPPLIER NUMBER: 11415415 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Circuit designers bucking VGA standards. (analysis of market for graphics controllers and developers' plans for them)
Ristelhueber, Robert
Chilton's Electronic News, v37, n1880, p1(3)
Sept 30, 1991
ISSN: 1054-6847 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2536 LINE COUNT: 00193

... escape the commodity status of current VGA devices.
Whereas until recently all application software was **written** to the VGA **register** -compatible **hardware** standard, the emergence of Windows is enabling software developer to write their programs directly to...

...now have more flexibility to create circuits that enhance the performance of Windows and other **graphical** user **interfaces** (**GUI**).
Some circuit designers contend that even before the emergence of Windows, the market had already...

11/3,K/7 (Item 7 from file: 275)

DIALOG(R)File 275:Gale Group Computer DB(TM)
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01449859 SUPPLIER NUMBER: 11233285 (USE FORMAT 7 OR 9 FOR FULL TEXT)
SVGA boards: fast enough for Windows, cheap enough for you. (Hardware Review) (overview of 21 evaluations of Super VGA graphics boards) (includes related articles on Editors' Choice, ATI Graphics Vantage board) (evaluation)
Flynn, Mary Kathleen; Kane, Robert W.
PC Magazine, v10, n16, p247(36)
Sept 24, 1991
DOCUMENT TYPE: evaluation ISSN: 0888-8507 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 5423 LINE COUNT: 00410

... CARES?
Thanks to Microsoft Windows, register compatibility is no longer an issue. Before VGA, most **graphics software** had been written to manipulate the video controller directly. This required a common **register** (**hardware**) standard, which IBM established with VGA. But IBM has yet to support Super VGA, which...

...This made it difficult for software vendors to support Super VGA because they had to **write** for a variety of **registers** .
Enter Windows. Software developers now **write** to the common environment rather than to a plethora of controllers. And for hardware vendors...

11/3,K/8 (Item 8 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01449398 SUPPLIER NUMBER: 11233357 (USE FORMAT 7 OR 9 FOR FULL TEXT)
ATI Technologies Inc.: ATI VGA Integra. (Hardware Review) (one of 21 evaluations of Super VGA boards in 'SVGA Boards: Fast Enough for Windows, Cheap Enough for You') (evaluation)
Poor, Alfred
PC Magazine, v10, n16, p270(2)
Sept 24, 1991
DOCUMENT TYPE: evaluation ISSN: 0888-8507 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 6643 LINE COUNT: 00483

... Thanks to Microsoft Windows, register compatibility is no longer an issue. Befor e VGA, most **graphics software** had been written to manipulate the video controlle r directly. This required a common **register** (**hardware**) standard, which IBM estab lished with VGA. But IBM has yet to support Super VGA...

...vendors to support Super VGA because they had to wri te for a variety of **registers** . Enter Windows. Software developers now **write** to the common environment rather th an to a plethora of controllers. And for hardware...

11/3,K/9 (Item 9 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01320230 SUPPLIER NUMBER: 07972118 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Sharing access to display resources in the Starbase/X11 Merge system.
Boyton, Jeff R.; Chakrabarti, Sankar L.; Hiebert, Steven P.; Lang, John J.; Owen, Jens R.; Marchington, Keith A.; Robinson, Peter R.; Stroyan, Michael H.; Waitz, John A.
Hewlett-Packard Journal, v40, n6, p20(13)
Dec, 1989
ISSN: 0018-1153 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 9180 LINE COUNT: 00694

... allowed to access the graphics hardware, and all other processes would actually be prevented from **accessing** the **registers** . This is not how the problem is solved in HP-UX. Instead, all processes are...

...convention be established and followed to ensure that only one process gains access to the **graphics display** at one time. The HP-UX kernel helps in this matter by providing a token...protocol of waiting to gain access to the token are not prevented from changing the **hardware registers** . The special kernel semaphore in the Starbase/X11 Merge system is often called the display...

11/3,K/10 (Item 10 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01249770 SUPPLIER NUMBER: 06747139 (USE FORMAT 7 OR 9 FOR FULL TEXT)
PCs crack the barrier to high-powered graphics. (includes related article on the IBM 8514-A PC graphics adapter)
Williams, Tom
Computer Design, v27, n11, p41(6)
June 1, 1988
ISSN: 0010-4566 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2921 LINE COUNT: 00229

... VGA chips.
Microfield has also done a microcoded X-server for the Unix-based X **Window** user **interface** . A server is the piece of code that presents a standard interface between Unix applications...

...sending it to a DOS window running under X. Even those "badly behaved" applications that **write** directly to **hardware registers** could be handled and displayed, according to Mallicoat. Beyond that, he says, there could conceivably...

11/3,K/11 (Item 11 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01120073 SUPPLIER NUMBER: 00644204
Programming the Enhanced Graphics Adapter.
Wilton, R.
Byte, v10, n11, p209-213
Fall, 1985
ISSN: 0360-5280 LANGUAGE: ENGLISH RECORD TYPE: ABSTRACT

...ABSTRACT: EGA) from IBM has many of the features that programmers wished its predecessor, the Color- **Graphics Monitor** Adapter (CGA), would have had. It generates sixteen-color bit-mapped raster graphics at a...

...the documentation is poor, which makes programming the device difficult. Topics covered include CGA compatibility, **hardware configurations** , graphics chip ports and **registers** , EGA RAM architecture, bit planes and pixels, writing a pixel, reading a pixel, and pixels...

11/3,K/12 (Item 1 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

01891445 Supplier Number: 54804873 (USE FORMAT 7 FOR FULLTEXT)
Cornerstone Announces ExtendYourStore(TM) Application Suite; Applications for In-Store and Web-based Customer and Transaction Data.
PR Newswire, p3582
June 7, 1999
Language: English Record Type: Fulltext

Document Type: Newswire; Trade
Word Count: 448

... engine/framework environment, each application can be deployed in a variety of operating system and **hardware** environments, across traditional **register / PC configurations** , over network computing **devices** , as well as via most **browsers** . This provides a single application environment to deliver consistent functionality and customer service at the...

11/3,K/13 (Item 2 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

01824568 Supplier Number: 54064808 (USE FORMAT 7 FOR FULLTEXT)
Schlumberger Selects POS Systems as Distributor and Service Provider for MagIC Point-of-sale Terminals in North America.
Business Wire, p1139
March 10, 1999
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 880

... memory, which can easily be upgraded. It interfaces with a wide range of peripherals, including **check** readers and electronic cash **registers** . The MagIC 6000 **terminal** also features a **graphic display** for user-friendly menus, and incorporates a graphical printer with rapid drop-in paper-roll...

11/3,K/14 (Item 3 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

01824551 Supplier Number: 54062026 (USE FORMAT 7 FOR FULLTEXT)
Schlumberger Celebrates North American Launch of MagicTM 6000 POS Terminals With Large-scale Smart Card Promotion At ETA Conference.
Business Wire, p1129
March 10, 1999
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 809

... memory, which can easily be upgraded. It interfaces with a wide range of peripherals, including **check** readers and electronic cash **registers** . The MagIC 6000 **terminal** features a **graphic display** which allows user friendly menus, and incorporates a fast graphical printer with rapid drop-in...

11/3,K/15 (Item 4 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

01502365 Supplier Number: 47202343 (USE FORMAT 7 FOR FULLTEXT)
Seven Major P-O-S Vendors Integrate Insignia Systems' Stylus Select
PR Newswire, p311MNTU003
March 11, 1997
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 380

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
...POS applications. "Point-Of-Sale" refers to the software and systems that control the cash **registers** and **scanners** at the front lane checkouts in retail stores. Six of the seven (ACR, Bass, Innovax...

...Providers, S4 and TCI, are industry leaders focusing on supermarket POS systems solutions. The seventh, **CAM** Data, is an industry leader focusing its solutions on general retailing. For Stylus sales, these...

11/3,K/16 (Item 1 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

04513558 Supplier Number: 58122927 (USE FORMAT 7 FOR FULLTEXT)
BANK OF NEW YORK UPGRADES BROWSER SERVICE.
Corporate EFT Report, v19, n24, pNA
Dec 8, 1999
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 125

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
The Bank of New York (BK), with $63 billion in assets, has introduced **check** imaging capabilities to CA$H- **Register** Plus, its **browser** -based cash management service. The addition of check imaging enables the bank's clients to retrieve and display images of check information directly from their **browser** . The service offers high- quality check images, as compared to microfilm or photocopies, bank officials...

...Check images are available at all times and are accessible from multiple sites within the **client** 's organization. CA$H- **Register** Plus corporate users also can schedule and retrieve account information, execute free-form and

11/3,K/17 (Item 2 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

03694461 Supplier Number: 47969931 (USE FORMAT 7 FOR FULLTEXT)
SOYO: SOYO launches two new mainboards for PC97
M2 Presswire, pN/A
Sept 10, 1997
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 691

... to hard disk for system resume.
Access to BIOS settings can be made via a **graphical** user **interface** under Windows 95, with natural language descriptions to help the user make the best choice where options are available. In addition, an automatic optimisation function can resolve **hardware** **configuration** down to the **register** level.
Built-in monitoring allows the system to provide a 'health' report of a number...

11/3,K/18 (Item 3 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

03199375 Supplier Number: 46556548 (USE FORMAT 7 FOR FULLTEXT)
A Do-Everything Back Office Package That Doesn't
Law Office Technology Review, v5, n7-7, pN/A
July 19, 1996
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 1188

... amount billed and amount of unbilled work. The Checkbook window can be split between a **check** **register** and a data entry form which **cam** be

set, on the fly, for check, deposit, ATM transaction, inter-account transfer, or payroll...

...the Billing window, the data entry portion also documents the transaction line selected from the **register** list.
The **Client** window has a client list on top and can have a client data entry screen...

11/3,K/19 (Item 4 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

02809671 Supplier Number: 45700137 (USE FORMAT 7 FOR FULLTEXT)
FPGA DESIGN SYNTHESIS
Computer Aided Design Report, v5, n8, pN/A
August, 1995
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 3647

... understand the design synthesis process. Here is a brief review.
1. To begin the process, **write** what is commonly called a " **register** -transfer -level" (RTL) **hardware** description language program describing the functions of the circuit. This task may be undertaken with...

...tools, including an ordinary text editor, an intelligent editor that understands HDL structure, or a **graphical** code generating **program** that produces HDL from state charts or block diagrams. (Such graphical editors are available from...

11/3,K/20 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

07885568 Supplier Number: 65863667 (USE FORMAT 7 FOR FULLTEXT)
Checkout on the fly.(Brief Article)
Ukens, Carol
Drug Topics, v144, n19, p77
Oct 2, 2000
Language: English Record Type: Fulltext
Article Type: Brief Article
Document Type: Magazine/Journal; Trade
Word Count: 74

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
...scan purchases of customers in line and print out a bar code that is then **scanned** at the cash **register** to complete the sale. The **device** is the latest addition to the ExtendYourStore suite from Austin-based 360Commerce. Unleashed is a server-centric Java application that runs on Palm OS with a **browser** interface. For more information, go to www.360Commerce.com.

11/3,K/21 (Item 2 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

04766238 Supplier Number: 47016210 (USE FORMAT 7 FOR FULLTEXT)
Shrunken emulator fits on desktop
Electronic Engineering Times, p18
Jan 6, 1997
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 161

SuperTAP 860 includes a 32-kbyte real-time trace, trace disassembler, CPU register **browser** and real-time event detection. The trace-and-disassembler system allows users to watch software...

...and debug code as it runs in the processor's cache in real-time. The **browser** provides an on-screen view into the state and capability of the MPC860's 200-odd **registers** , helping to **configure** the integrated **peripherals** .

A SuperTAP 860 system with 25-MHz support, 32-kbyte trace, 1-Mbyte overlay memory...

11/3,K/22 (Item 3 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

02858243 Supplier Number: 43848701 (USE FORMAT 7 FOR FULLTEXT)
Font rendering has added risc character
Electronics Times, p10
May 20, 1993
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 233

... inter-unit bus is a bi-directional data bus by which the cpu sets and **reads** values in **registers** of other **units** . The main external interfaces are for data transfers with instruction memory, data memory and graphic memory. The **graphic** memory **interface** is split from the data memory interface so the cpu can access font data while...

11/3,K/23 (Item 4 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

01884566 Supplier Number: 42394200 (USE FORMAT 7 FOR FULLTEXT)
Circuit Designers Bucking VGA Standards
Electronic News (1991), p1
Sept 30, 1991
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 2395

... escape the commodity status of current VGA devices.

Whereas until recently all application software was **written** to the VGA **register** -compatible **hardware** standard, the emergence of Windows is enabling software developer to write their programs directly to...

...now have more flexibility to create circuits that enhance the performance of Windows and other **graphical** user **interfaces** (**GUI**).

Some circuit designers contend that even before the emergence of Windows, the market had already...

11/3,K/24 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

12905169 SUPPLIER NUMBER: 68146149 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Processor adds encryption to a PC. (Hardware Review) (Evaluation)
Cravotta, Nicholas
EDN, 45, 24, 20
Nov 23, 2000
DOCUMENT TYPE: Evaluation ISSN: 0012-7515 LANGUAGE: English
RECORD TYPE: Fulltext
WORD COUNT: 737 LINE COUNT: 00065

... processing interface) for interacting with an Embassy service and

the Embassy Manager, which presents a **graphical** user **interface** for basic administrative tasks, including initial registration, an interface into the transaction engine, and a...

...all communications between the processor and WaveNet by communicating through a WaveNet transaction gateway to **register** a **processor** or to **fetch** keys.

Processors must be registered to establish their identities for subsequent authorization to load a...

11/3,K/25 (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

11755371 SUPPLIER NUMBER: 54060511 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Product Locator.(Buyers Guide)
Appliance Manufacturer, 46, 12, PL-1(1)
Dec, 1998
DOCUMENT TYPE: Buyers Guide ISSN: 0003-679X LANGUAGE: English
RECORD TYPE: Fulltext
WORD COUNT: 36357 LINE COUNT: 09342

... GM Nameplate, Inc., North Carolina
Magna Plan Corp.
Panduit Corp.
Software Co-Op, Inc.
Standard **Register**
Tyton Hellermann
Weber Marking Systems, Inc.

Micro Computers

Control Concepts, Inc., Matrin Technologies
EMS, Elektromotoren...
...Plotters

BRADY Worldwide, Inc., Identification Solutions Division
* Omega Engineering, Inc.
Software Co-Op, Inc.
Standard **Register**
Summagraphics Corporation
U.V. Process Supply, Inc.

Process Control

Analogic Corp., Measurement & Control Division (MCD...BP America Plastec, BP America Chemicals Company
Broadview Injection Molding Co., Inc.
Bruce Plastics, Inc.
CAE Services Corp.
Caldwell Industries, Inc.
Carlisle Engineered Products
Casco Plastics
Cavallero Plastics Inc.
Chardon Rubber...

...Div.
ARRK Creative Network Corp., United States
Bel-Art Products
Broadview Injection Molding Co., Inc.
CAE Services Corp.
Chardon Rubber Co.
Davies Molding L.L.C.

Dimco-Gray Co.
Elmec Products...Corp.
Cadillac Plastic & Chemical Co.
Dynacast
Ferro Corp., Plastic Colorants & Dispersions Division
Foster Corporation

Analysis

CAE Services Corp.

Cellulosic

Cadillac Plastic & Chemical Co.
Dow U.S.A.
Dynacast
* Eastman Chemical Company...

11/3,K/26 (Item 3 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

09812303 SUPPLIER NUMBER: 19921612 (USE FORMAT 7 OR 9 FOR FULL TEXT)
SuperTAP(TM) 860T and SuperTAP 860SAR Emulators Now Available From Applied Microsystems
PR Newswire, p1027SFM084
Oct 27, 1997
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 681 LINE COUNT: 00063

... with 8 MB configurations with one wait-state at 50MHz.
With the on-line visual **register browser** too), engineers can quickly **configure** and save the content of the **processor** 's integrated CPM **registers** , The event system enables real-time detection of events in the target system and high...

11/3,K/27 (Item 4 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

09325046 SUPPLIER NUMBER: 19099437 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Competing trends fuel the drive toward leak detection compliance. (includes related article on Veeder-Root's Simplicity Petroleum Data Services program)
Bishop, Jim
National Petroleum News, v88, n13, pS14(7)
Dec, 1996
ISSN: 0149-5267 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 5976 LINE COUNT: 00484

... early 1997, takes advantage of a station's existing onsite computer capabilities and adds the **GUI** interface to simplify use by the station operator, DeBlock notes. "Since (the owner) has made...

...investment in a PC that's already onsite and that utilizes a scanning program to **scan** items into the cash **register** , now that same **PC** can be used to operate the compliance unit or the fuel management unit outside by making the **graphical** user **interface** very simple for the operator to use," he explains.
The system enables operators to view...

11/3,K/28 (Item 5 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

08102477 SUPPLIER NUMBER: 17296229 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Content addressable memory.
Weldon, Tom
EDN, v40, n14A, p13(2)
July 17, 1995
ISSN: 0012-7515 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 2401 LINE COUNT: 00189

... may also be masked out of a comparison by using one of the two mask **registers** .
The **device** has a very simple interface, as seen from the logic symbol in Figure 3. Four...

...DQ) is multiplexed up to four ways to access the 64-bit internal architecture. Internal **configuration registers** give the user control over which 16-bit segments are used; for example, a 48...

11/3,K/29 (Item 6 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
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07592611 SUPPLIER NUMBER: 16497910 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Configurable address processor does matching in 80 ns. (Kawasho International's KE5B061A1 memory chip) (New Products) (Product Announcement)
Bursky, Dave
Electronic Design, v42, n24, p159(1)
Nov 21, 1994
DOCUMENT TYPE: Product Announcement ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 859 LINE COUNT: 00066

... KE5B064A1s can be cascaded to enlarge the table size until the higher-capacity chips are **ready** . The internal **registers** of the address **processor** chip were designed to allow expansion--hit registers and status registers across all cascaded chips work with each other, creating one large **CAM** with no additional external logic.
Kawasho designers created an evaluation system that includes an evaluation...

11/3,K/30 (Item 7 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
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07269945 SUPPLIER NUMBER: 15485739 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Computerization, green issues focus of Italian show. (GEC '94, an international exhibition for converting, printing, publishing and paper industries to be held in Milan, Italy) (Special Paper, Film and Foil Converter Editorial Report)
Paper, Film & Foil Converter, v68, n5, p131(3)
May, 1994
ISSN: 0031-1138 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 2872 LINE COUNT: 00242

... color-registration and the CR8-LT for ribbon-registration. The CR11 for automatic longitudinal color- **register** control and the Grafikscan web **scanner** will be unveiled. On display will be the CR7-LT for color-register control for rotogravure presses, COVISTA/F viscometer and **CAM** 2 automatic ink-feeding equipment for rotogravure presses.
Halm Industries International Co. Inc., Warmond, Holland...

11/3,K/31 (Item 8 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2003 The Gale Group. All rts. reserv.

06484148 SUPPLIER NUMBER: 13995992 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Integration: the future of instrumentation.
House, Richard
Automotive Engineering, v101, n3, p13(5)
March, 1993
ISSN: 0098-2571 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2745 LINE COUNT: 00233

... often ASCII data, to the driver--which then sends this over the bus to the **instrument** .
The **registers** of plug-in data- **acquisition** boards and VXI instruments are programmed directly by the driver. The more sophisticated data-acquisition...

11/3,K/32 (Item 9 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2003 The Gale Group. All rts. reserv.

05537930 SUPPLIER NUMBER: 11600162 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Graphics board makers anoint Microsoft; but IBM's register-conscious graphics modes will live on as developers tie in to the CPU bus. (Microsoft Corp's Windows graphical user interface is standard of choice for board makers at the Comdex Fall 1991 trade show)
Harbert, Tammi
EDN, v36, n21A, p1(2)
Oct 17, 1991
ISSN: 0012-7515 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1443 LINE COUNT: 00116

...ABSTRACT: handle higher resolutions and speed graphics processing. Traditional methods for attaining higher graphics performance involve **writing** directly to the **hardware registers** of graphics controller chips. Today, Windows 3.0 and similar **GUIs** allow developers to write to standard software interfaces, which frees board makers from register-based ...
... New options
In the past, the best way to attain high graphics performance was to **write** directly to the **hardware registers** of graphics controller chips, such as those for VGA. That fact made adherence to **register** -based **hardware** standards critical. But today, with application interfaces available for Windows 3.0 and the **graphical** user **interfaces** like it, application developers write to standard software interfaces. Thus board vendors, so long as they provide good **graphical** user- **interface** drivers, are essentially free of register-based standards.
Instead, many board vendors are either developing...

11/3,K/33 (Item 10 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
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04793766 SUPPLIER NUMBER: 08761892 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Intelligent cards display megapixels; TIGA 340X0-based graphics boards. (graphics boards based on Texas Instruments' 34010 and 34020 microprocessors and the Texas Instruments Graphics Architecture) (includes related article comparing the TIGA 340X0 and IBM's 8514/A)
Wright, Maury
EDN, v35, n16, p81(6)
August 2, 1990
ISSN: 0012-7515 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 3460 LINE COUNT: 00285

... will run on TIGA boards. You can expect more applications in the future, however, that **write** directly to 8514/A **hardware registers** . Third-party vendors have also added compatibility to 340X0-based boards. GSS (**Graphics Software** Systems), for example, licenses its DGIS

graphics standard for use on 34OX0 boards. The company...

11/3,K/34 (Item 11 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

03283837 SUPPLIER NUMBER: 05071647 (USE FORMAT 7 OR 9 FOR FULL TEXT)
What's new for the future in supermarket technology?
Shulman, Richard E.
Supermarket Business, v42, p20(2)
July, 1987
ISSN: 0196-5700 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 1654 LINE COUNT: 00130

... The screen guides the customer in performing all the checkout activities. It switches from a **computer** graphic **display** of **register tape** and special action "keys' to a laser disk projection of a woman who "speaks' to...

11/3,K/35 (Item 12 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

02324965 SUPPLIER NUMBER: 03701834 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Programmable controller update; a guide to specifications.
Donovan, John
Plant Engineering, v39, p44(20)
March 28, 1985
ISSN: 0032-082X LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 5142 LINE COUNT: 00419

... asking for it by name. A spreadsheet allows calculations to be performed on data from **PC registers** and can send the results to these registers as well. Users can set alarms, **monitor** or force coils and **registers** , time events, **access** and control PID loops, convert, analog data to bar graphs, and produce custom **graphic displays** to show real-time process status. The software supports PCs from Allen-Bradley, General Electric...

11/3,K/36 (Item 1 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

01979585 46271199
Regulating e-commerce: Formal transactions in the digital age
Murray, Andrew D; Vick, Douglas W; Wortley, Scott
International Review of Law, Computers & Technology v13n2 PP: 127-145
Aug 1999
ISSN: 1360-0869 JRNL CODE: IRLC
WORD COUNT: 11396

...TEXT: by solicitors with the option of printing results with a RoS watermark from a local **printer** . This new system, called ' **Registers** Direct', makes use of **browser** technology. This means any office or home with an Internet connection can make use of...

...to a minimum as users will only have to pay the standard search cost for **access** to the **register** .75 The entire system is protected by firewalls at key stages and will allow **access** to all RoS **registers** -the Land Register, the Sasine Register76 and the Register of Inhibitions and Adjudications.77 The...

11/3,K/37 (Item 2 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

00917438 95-66830
Newstrack
Fox, Robert
Communications of the ACM v37n10 PP: 9-10 Oct 1994
ISSN: 0001-0782 JRNL CODE: ACM
WORD COUNT: 1045

...TEXT: the service up to other industries and governmental groups," said a spokesperson for Nynex.

SPEEDY **CHECK** -OUTS...A **computer** -based cash **register** is being manufactured to help make the supermarket check-out process more pleasant for shoppers...

... Pa., is powered by an Intel i486 microprocessor that runs special software based on a **Window** 's **interface** and has the ability to display pictures of products for easy identification and pricing. An...

11/3,K/38 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2003 CMP Media, LLC. All rts. reserv.

01220648 CMP ACCESSION NUMBER: EET20000807S0057
Regent register-creation tool expands to include software designers
Richard Goering
ELECTRONIC ENGINEERING TIMES, 2000, n 1125, PG58
PUBLICATION DATE: 000807
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: DESIGN AUTOMATION
WORD COUNT: 390

Regent provides a **graphical** user **interface** that lets **hardware** and system designers describe system **registers** . Users enter information like **register** names, addresses and **access** attributes. Users also specify the bus interface. The tool supports standard buses like ARM Ltd ...

11/3,K/39 (Item 2 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2003 CMP Media, LLC. All rts. reserv.

01115507 CMP ACCESSION NUMBER: EET19970106S0031
Shrunken emulator fits on desktop
ELECTRONIC ENGINEERING TIMES, 1997, n 935, PGP20
PUBLICATION DATE: 970106
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Product File - Test & Measurement
WORD COUNT: 169

SuperTAP 860 includes a 32-kbyte real-time trace, trace disassembler, CPU register **browser** and real-time event detection. The trace-and-disassembler system allows users to watch software...

...and debug code as it runs in the processor's cache in real-time. The **browser** provides an on-screen view into the state and capability of the MPC860's 200-odd **registers** , helping to **configure** the integrated **peripherals** .
A SuperTAP 860 system with 25-MHz support, 32-kbyte trace, 1-Mbyte overlay memory...

11/3,K/40 (Item 3 from file: 647)

DIALOG(R)File 647:CMP Computer Fulltext

00596635 CMP ACCESSION NUMBER: CWK19910429S1968
Symmetry 2000 Connectivity Products
COMMUNICATIONSWEEK INTERNATIONAL, 1991, n 063, 21
PUBLICATION DATE: 910429
JOURNAL CODE: CWI LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: USER NETWORKING - Product Briefs
WORD COUNT: 679

... Disoss and Digital Equipment Corp.'s All-in-One. PC FTAM client software enables any **PC** to **retrieve** data from **registers** or databases held on minicomputers or mainframes, using File Transfer Access Management. * PRICE: Depends on...

...letters to indexed documentation. The product is Windows-based and is combined with a vector **graphics program** . It runs on Sinix, SNI's version of Unix. * PRICE: On application. * AVAILABILITY: Immediately. Etherlink...

11/3,K/41 (Item 1 from file: 674)
DIALOG(R)File 674:Computer News Fulltext

082957
Neoware debuts thin version of Linux
Byline: APRIL JACOBS
Journal: Network World Page Number: 14
Publication Date: April 10, 2000
Word Count: 400 Line Count: 37

Text:
... clients and can also be used for specific application boxes such as corporate security card **readers** , cash **registers** and firewall **devices** .In conjunction with its release of NeoLinux, Neoware debuted a thin client dubbed Eon, or...

... ICA protocol, which lets users access applications for the Windows platform. A Netscape Navigator Web **browser** and Java Virtual Machine are provided for Internet environments.Eon has an integrated National Semiconductor...

11/3,K/42 (Item 1 from file: 369)
DIALOG(R)File 369:New Scientist

00100987 14219213.500 (USE FORMAT 7 OR 9 FOR FULLTEXT)
The future of work: it's all in the mind - In a world where offices cease to exist and job security has gone the way of lamplighters, your most precious asset will be your intelligence
ARTHUR, CHARLES
New Scientist, vol. 142, no. 1921, p. Page 28
April 16, 1994
LANGUAGE: English RECORD TYPE: Fulltext DOC. TYPE: Journal
WORD COUNT: 2960

(USE FORMAT 7 OR 9 FOR FULLTEXT)

TEXT:
...speed data networks); Answering machines (computers); Insurance claims assessors (neural networks); Bailiffs (electronic credit freezes); **Checkout** staff (image recognition software); Cash **register** suppliers (**computers**); Coal & solid fuel merchants (electricity); Company registration agents (networks); Dictation & secretarial services (voice

•recognition software...

...Industrial relations arbitrators (employment deregulation); Notaries and commissioners of oaths (video recordings); Draughting equipment makers (**computer - aided design**); Typewriter manufacturers (computers); Window cleaners (intelligent robots); Airlines (rising fuel prices); Middle managers (networks)

File 347:JAPIO Oct 1976-2003/Mar(Updated 030703)
(c) 2003 JPO & JAPIO
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200348
(c) 2003 Thomson Derwent
File 348:EUROPEAN PATENTS 1978-2003/Jul W03
(c) 2003 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20030724,UT=20030717
(c) 2003 WIPO/Univentio

Set	Items	Description
S1	1479	AU=(KING J? OR ROGERS S?)
S2	12	S1 AND REGISTER? ?/TI,AB
S3	11	S2 AND IC=(G09G OR G06F)

3/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2003 Thomson Derwent. All rts. reserv.

014877236 **Image available**
WPI Acc No: 2002-697942/200275
XRPX Acc No: N02-550383
Graphical program creating method for accessing registers **in hardware device involves executing graphical program during which** register **access node is operable to access** registers **of hardware device**
Patent Assignee: KING J S (KING-I); ROGERS S W (ROGE-I)
Inventor: **KING J S ; ROGERS S W**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020109726	A1	20020815	US 2000742523	A	20001220	200275	B

Priority Applications (No Type Date): US 2000742523 A 20001220
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020109726	A1		29	G09G-005/00	

Abstract (Basic): US 20020109726 A1
NOVELTY - A **register** access node in a graphical program is displayed on a screen, in response to user input. During execution of the graphical program, the **register** access node is operable to access **registers** of a hardware device.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(1) Memory medium storing program for accessing **registers** in hardware device; and
(2) **Register** accessing system.
USE - For creating a graphical program for accessing **registers** in hardware device.
ADVANTAGE - Direct read/write access to **register** , is gained without the need to write specific I/O drivers for the hardware device, hence reduces development time required to create graphical program and number of code defects in the graphical program.
DESCRIPTION OF DRAWING(S) - The figure shows flowchart of creating a graphical program.
pp; 29 DwgNo 5/12
Title Terms: GRAPHICAL; PROGRAM; METHOD; ACCESS; REGISTER; HARDWARE; DEVICE ; EXECUTE; GRAPHICAL; PROGRAM; REGISTER; ACCESS; NODE; OPERATE; ACCESS; REGISTER; HARDWARE; DEVICE
Derwent Class: P85; T01
International Patent Class (Main): **G09G-005/00**
File Segment: EPI; EngPI

3/5/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2003 Thomson Derwent. All rts. reserv.

014877234 **Image available**
WPI Acc No: 2002-697940/200275
XRPX Acc No: N02-550381
Data type information propagation method in graphical programming environment, involves transmitting information specifying hardware device with which register **access node is associated to another hardware device node**
Patent Assignee: KING J S (KING-I); ROGERS S W (ROGE-I)
Inventor: **KING J S ; ROGERS S W**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020109722	A1	20020815	US 2000742946	A	20001220	200275	B

Priority Applications (No Type Date): US 2000742946 A 20001220

Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20020109722 A1 29 G06F-003/00

Abstract (Basic): US 20020109722 A1
NOVELTY - A **register** access node operated to access a hardware device is connected to another **register** access node in response to user input. The information specifying the hardware device with which the **register** access node is associated is transmitted to the another hardware device node in response to the connection between both the nodes.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(1) Method for performing type checking for hardware device node in graphical program;
(2) Type information propagating system for hardware device nodes;
(3) Memory medium storing program instructions for propagating type information for hardware device nodes;
(4) System for propagating type information for hardware device nodes; and
(5) System for performing type checking for hardware device node.
USE - For propagating data type information for hardware device nodes in graphical programming environment.
ADVANTAGE - The direct read/write access to **registers** in hardware device is gained without need to write input-output drivers for the hardware device, hence the development time required to create graphical program is reduced and the number of node defects in the program are reduced.
DESCRIPTION OF DRAWING(S) - The figure shows a representative instrumentation control system.
pp; 29 DwgNo 1A/12
Title Terms: DATA; TYPE; INFORMATION; PROPAGATE; METHOD; GRAPHICAL; PROGRAM ; ENVIRONMENT; TRANSMIT; INFORMATION; SPECIFIED; HARDWARE; DEVICE; REGISTER; ACCESS; NODE; ASSOCIATE; HARDWARE; DEVICE; NODE
Derwent Class: T01
International Patent Class (Main): **G06F-003/00**
International Patent Class (Additional): **G06F-013/00**
File Segment: EPI

3/5/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008646274 **Image available**
WPI Acc No: 1991-150303/199121
XRPX Acc No: N91-115413
Matrix addressable display and driver having CRT compatibility - uses row driver circuits into individual shift register **and driver banks**
Patent Assignee: DELCO ELTRN CORP (DELC-N)
Inventor: **KING J F** ; VINCEN M R
Number of Countries: 004 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 428324	A	19910522	EP 90312187	A	19901107	199121	B

Priority Applications (No Type Date): US 89435917 A 19891113
Cited Patents: NoSR.Pub
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
EP 428324 A
Designated States (Regional): DE FR GB IT

Abstract (Basic): EP 428324 A
The matrix addressable display (100) includes N individually controlled red (R), green (G) and (B) pixels disposed at the intersections of a matrix array of vertically extending columns and laterally extending rows, grouped to define N/3 triads consisting of a

red, blue and green pixel.

The pixels in each row of the display are disposed in every other column and in a predefined, uniform colour sequence. The pixels in every other row are laterally shifted in both location and colour with respect to adjacent rows such that the pixels in each column are of the same colour. Each colour element is defined by a triad of pixels.

ADVANTAGE - Colour select circuitry is greatly simplified or eliminated. Drive signal compatibility with cathode ray tube graphics controllers. (8pp Dwg.No.3/3)

Title Terms: MATRIX; ADDRESS; DISPLAY; DRIVE; CRT; COMPATIBLE; ROW; DRIVE; CIRCUIT; INDIVIDUAL; SHIFT; REGISTER; DRIVE; BANK
Derwent Class: P85; T04
International Patent Class (Additional): **G09G-003/20**
File Segment: EPI; EngPI

3/5/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004491631
WPI Acc No: 1985-318509/198551
XRPX Acc No: N85-236740

Document scanning system with information-enhancement - multiplies values of pixels in window by predetermined constants and sums them to provide value for each sensed pixel

Patent Assignee: NCR CANADA LTD (NATC)
Inventor: ATAMAN E; **KING J T**
Number of Countries: 013 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 165045	A	19851218				198551	B
AU 8543142	A	19851219				198607	
ZA 8503805	A	19851126				198609	
JP 61045376	A	19860305				198616	
DK 8502660	A	19851215				198626	
US 4613986	A	19860923	US 84620660	A	19840614	198641	
EP 165045	B	19910220				199108	
DE 3581766	G	19910328				199114	
CA 1286394	C	19910716				199133	

Priority Applications (No Type Date): US 84620660 A 19840614
Cited Patents: 1.Jnl.Ref; A3...8750; No-SR.Pub; US 3973239; WO 8103096
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 165045	A	E	37		
Designated States (Regional): AT BE CH DE FR GB LI					
EP 165045	B				
Designated States (Regional): AT BE CH DE FR GB LI					

Abstract (Basic): EP 165045 A

A column of document sensors (16) is scanned to provide digital signals representative of pixel grey levels which are applied sequentially to a latch (55). The latch is coupled to the first of a sequentially coupled group of RAM's (40-43) addressed by a common address circuit (44). The apparatus has other latches (56-59) for input-output operations, the arrangement effecting a one scan line delay.

Outputs of the latches are applied to combining devices including sequences of adders, element delays and multipliers. For each sensed pixel the values of the pixels in a window are multiplied by predetermined constants and summed to provide an enhanced value for the sensed pixel. The window is shifted by one row for each sensed pixel.

ADVANTAGE - Uses simple digital fitter.

3/13

Title Terms: DOCUMENT; SCAN; SYSTEM; INFORMATION; ENHANCE; MULTIPLICATION; VALUE; PIXEL; WINDOW; PREDETERMINED; CONSTANT; SUM; VALUE; SENSE; PIXEL
Derwent Class: W02
International Patent Class (Additional): **G06F-000/00** ; G06K-009/36;

H03H-017/02; H04N-001/40
File Segment: EPI

3/5/5 **(Item 5 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
(c) 2003 Thomson Derwent. All rts. reserv.

004308113
WPI Acc No: 1985-134991/198523
XRPX Acc No: N85-101505
Test and maintenance apparatus for data processor - responds to external control signals by shifting data into and out of registers **independently of processor operation**
Patent Assignee: HONEYWELL INFORM SYSTEMS INC (HONE)
Inventor: **KING J L**
Number of Countries: 012 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
AU 8433381	A	19850418	AU 8433381	A	19840921	198523	B
NO 8403375	A	19850506				198525	
EP 145866	A	19850626	EP 84111641	A	19840928	198526	
FI 8403878	A	19850407				198530	

Priority Applications (No Type Date): US 83539355 A 19831006
Cited Patents: 2.Jnl.Ref; A3...8804; EP 31501; No-SR.Pub; US 3790885; US 4167780
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
AU 8433381	A		42		
EP 145866	A	E			

Designated States (Regional): BE CH DE FR GB IT LI NL SE

Abstract (Basic): AU 8433381 A

The apparatus consists of a number of coupled **register** cells. A group of the cells are adapted to receive data signals from an associated group of **registers** of the data processing system. A second group of the **register** cells are adapted to apply data signals from a second associated group of **register** cells of the data processing system.

External control signals are used for shifting data signals into and out of the **register** cells independent of the operation of the data processing system. The first group of **register** cells are prevented from receiving data signals and from applying and data signals to the second group of cells during shifting of data signals into and out of the cells.

ADVANTAGE - Data signals can be entered or extracted without halting operation of data processing system.

0/12

Title Terms: TEST; MAINTAIN; APPARATUS; DATA; PROCESSOR; RESPOND; EXTERNAL; CONTROL; SIGNAL; SHIFT; DATA; REGISTER; INDEPENDENT; PROCESSOR; OPERATE
Derwent Class: S01; T01
International Patent Class (Additional): **G06F-011/00**
File Segment: EPI

3/5/6 **(Item 6 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
(c) 2003 Thomson Derwent. All rts. reserv.

004308112
WPI Acc No: 1985-134990/198523
XRPX Acc No: N85-101504
Test and maintenance system for data processor - enters preselected data signal into registers **to be tested and compares output with expected output**
Patent Assignee: HONEYWELL INFORM SYSTEMS INC (HONE)
Inventor: **KING J L** ; MILLER H W

Number of Countries: 013 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
AU 8433380	A	19850418	AU 8433380	A	19840921	198523	B
NO 8403374	A	19850506				198525	
EP 146698	A	19850703	EP 84111613	A	19840928	198527	
FI 8403879	A	19850407				198530	
US 4581738	A	19860408				198617	
CA 1219376	A	19870317				198715	
KR 9205233	B1	19920629	KR 846182	A	19841005	199401	

Priority Applications (No Type Date): US 83539357 A 19831006
Cited Patents: 2.Jnl.Ref; A3...8802; No-SR.Pub; US 4298980
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
AU 8433380	A		38		
EP 146698	A	E			
Designated States (Regional): BE CH DE FR GB IT LI NL SE					
KR 9205233	B1			G06F-011/26	

Abstract (Basic): AU 8433380 A
The appts. provides a predetermined signal group to a data processing system, and has a clock signal distribution device controlled by selected signals in the signal group. The appts. also includes a number of logic component groups, each component group having a number of **registers** . The **registers** have a mode for normal data processing system operation, and a second mode for test and maintenance operations.
An addressing device responds to preselected signals of the signal group, causing a preselected component group to be in the second mode, the predetermined signal groups being stored in the **registers** .
0/11
Title Terms: TEST; MAINTAIN; SYSTEM; DATA; PROCESSOR; ENTER; PRESELECTED; DATA; SIGNAL; REGISTER; TEST; COMPARE; OUTPUT; OUTPUT
Derwent Class: T01
International Patent Class (Main): **G06F-011/26**
File Segment: EPI

3/5/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003963680
WPI Acc No: 1984-109224/198418
XRPX Acc No: N84-080809
Operating system supervisor for data processor system - identifies fault condition in system requiring different operating system and addresses reserved memory area of current system
Patent Assignee: HONEYWELL INFORM SYSTEMS INC (HONE)
Inventor: ANGELLE P A; **KING J L** ; PORTER M G
Number of Countries: 014 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 106669	A	19840425	EP 83306193	A	19831013	198418	B
AU 8318931	A	19840419				198423	
FI 8303639	A	19840531				198428	
ES 8406758	A	19841101				198503	
US 4493034	A	19850108	US 82434344	A	19821014	198504	
CA 1193739	A	19850917				198542	
EP 106669	B	19900418				199016	
DE 3381475	G	19900523				199022	

Priority Applications (No Type Date): US 82434344 A 19821014
Cited Patents: 1.Jnl.Ref; A3...8701; EP 24434; EP 93267; No-SR.Pub; US 4253145
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes

EP 106669 A E 18
Designated States (Regional): BE CH DE FR GB IT LI NL SE
EP 106669 B
Designated States (Regional): BE CH DE FR GB IT LI NL SE

Abstract (Basic): EP 106669 A
The supervisor procedures react to certain conditions in a CPU e.g. a supervisor clock reaching a predetermined count to enter a set of signals indicating a condition in a fault **register** . The signals in the fault **register** are compared with signals previously entered in the supervisor fault enable **register** . When a coincidence is detected, a different operating system is activated. The contents of **registers** defining the state of the CPU under the current operating system is safely stored in a reserve memory area in a memory unit associated with that operating system.
Information defining the required fresh state of the CPU associated with the new operating system is read into the **registers** . The CPU quantities relating to the address of the reserve memory area associated with the current operating system is entered into the **register** . The fresh operating system is initiated and execution of permitted instructions by the second system is begun. Physical memory locations are determined by a real address via use of a paying mechanism.
Title Terms: OPERATE; SYSTEM; SUPERVISION; DATA; PROCESSOR; SYSTEM; IDENTIFY; FAULT; CONDITION; SYSTEM; REQUIRE; OPERATE; SYSTEM; ADDRESS; RESERVE; MEMORY; AREA; CURRENT; SYSTEM
Derwent Class: T01
International Patent Class (Additional): **G06F-009/44** ; **G06F-012/16**
File Segment: EPI

3/5/8 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00131742
Test and maintenance system and method for a data processing system.
Pruf- und Wartungssystem und -verfahren fur Datenverarbeitungssystem.
Systeme et methode de test et de maintenance pour systeme de traitement de donnees.
PATENT ASSIGNEE:
Honeywell Information Systems Inc., Honeywell Plaza, Minneapolis Minnesota 55408, (US), (applicant designated states: BE;CH;DE;FR;GB;IT;LI;NL;SE)
INVENTOR:
King, James L. , 1251 West Rancho Drive, Phoenix Arizona 85013, (US
LEGAL REPRESENTATIVE:
Falcetti, Carlo , Servizio Brevetti Honeywell I.S.I., I-20010 Pregnana Milanese, (IT)
PATENT (CC, No, Kind, Date): EP 145866 A2 850626 (Basic)
EP 145866 A3 880127
APPLICATION (CC, No, Date): EP 84111641 840928;
PRIORITY (CC, No, Date): US 539355 831006
DESIGNATED STATES: BE; CH; DE; FR; GB; IT; LI; NL; SE
INTERNATIONAL PATENT CLASS: **G06F-011/26**
CITED PATENTS (EP A): EP 231501 A; US 3790885 A; US 4167780 A
CITED REFERENCES (EP A):
IBM TECHNICAL DISCLOSURE BULLETIN, vol. 17, no. 7, December 1974, pages 1941-1944, New York, US; L.D. HOWE et al.: "Troubleshooting large-scale integrated circuit units"
1978 IEEE SEMICONDUCTOR TEST CONFERENCE, Cherry Hill, New Jersey, 31st October - 2nd November 1978, pages 152-158, IEEE; J.H. STEWART et al.: "Application of scan/set for error detection and diagnostics";

ABSTRACT EP 145866 A2
Test and maintenance system and method for a data processing system.
A test and maintenance system for use with a data processing system comprising a specialized circuit set wherein the circuit set **registers**

can be configured into a serial array, a clock signal distribution system capable of delivering controlled clock signals to selected serial arrays, a maintenance data processor for providing predetermined signal groups, and addressing apparatus responsive to the predetermined signal groups for loading and unloading **register** arrays in response to the pre-determined signals. The disclosed apparatus permits a predetermined signal group to be entered into the serial **register** array, in a predetermined number of clock cycles (i.e. series of operations performed on the data), shifting of the resulting signals from the serial **register** array and signals outputting to data processing unit for display or analysis. By comparing the expected result for a given initial state with the actual result of an operation sequence, the accuracy of the operation of a data processing system, or any portion thereof, can be established. The test and maintenance system includes a group of **registers** and **register** cells through which data signals can be serially shifted. The serially coupled **registers** and **register** cells are coupled to active **registers** of the data processing systems and data signals can be extracted from or entered into the data processing system while the system is in operation. In this manner, the status of the system can be determined or control signals can be entered into the data processing system without halting operation.
ABSTRACT WORD COUNT: 257

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 850626 A2 Published application (Alwith Search Report ;A2without Search Report)
Search Report: 880127 A3 Separate publication of the European or International search report
Withdrawal: 880914 A2 Date on which the European patent application was deemed to be withdrawn: 871001
LANGUAGE (Publication,Procedural,Application): English; English; English

3/5/9 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00131714
Test and maintenance system for a data processing system.
Pruf- und Wartungssystem fur ein Datenverarbeitungssystem.
Systeme de test et de maintenance pour un systeme de traitement de donnees.
PATENT ASSIGNEE:
Honeywell Information Systems Inc., Honeywell Plaza, Minneapolis Minnesota 55408, (US), (applicant designated states: BE;CH;DE;FR;GB;IT;LI;NL;SE)
INVENTOR:
Miller, Homer W., 6904 West Corrine Drive, Peoria Arizona 85345, (US)
King, James L. , 1251 West Rancho Drive, Phoenix Arizona 85013, (US
LEGAL REPRESENTATIVE:
Falcetti, Carlo (42243), Bull HN Information Systems Italia S.p.A. Direzione Brevetti, I-20010 Pregnana Milanese (Milano), (IT)
PATENT (CC, No, Kind, Date): EP 146698 A2 850703 (Basic)
EP 146698 A3 880113
APPLICATION (CC, No, Date): EP 84111613 840928;
PRIORITY (CC, No, Date): US 539357 831006
DESIGNATED STATES: BE; CH; DE; FR; GB; IT; LI; NL; SE
INTERNATIONAL PATENT CLASS: **G06F-011/26**
CITED PATENTS (EP A): US 4298980 A
CITED REFERENCES (EP A):
DIGEST OF PAPERS OF THE 1979 IEEE TEST CONFERENCE, Cherry-Hill, New Jersey, 23rd-25th October 1979, pages 29-36, IEEE, New York, US; L.A. STOLTE et al.: "Design for testability of the IBM system/38"
PROCEEDINGS OF THE NATIONAL ELECTRONICS CONFERENCE, vol. 36, 1982, pages 346-350, Oak Brook, Illinois, US; S. AL-HARIRI et al.: "An easily testable structure for LSI and VLSI circuits";

ABSTRACT EP 146698 A2
Test and maintenance system for a data processing system.

A test and maintenance system for use with a data processing system comprising a specialized circuit set wherein the circuit set **registers** can be configured into a serial array, a clock signal distribution system capable of delivering controlled clock signals to selected serial arrays, a maintenance data processor for providing predetermined signal groups, and addressing apparatus responsive to the predetermined signal groups for loading and unloading **register** arrays in response to the predetermined signals. The disclosed apparatus permits a predetermined signal group to be entered into the serial **register** array, a predetermined number of clock cycles (i.e. series of operations performed on the data), and the resulting signals shifted from the serial **register** array and signals applies to data processing unit for display or analysis. By comparing the expected result for a given initial state with the actual result of an operation sequence, the accuracy of the operation of a data processing system, or any portion thereof, can be established.
ABSTRACT WORD COUNT: 171

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	850703 A2	Published application (Alwith Search Report ;A2without Search Report)
Change:	850731 A2	Title of invention (German) (change)
Change:	850731 A2	Title of invention (French) (change)
Search Report:	880113 A3	Separate publication of the European or International search report
Examination:	880907 A2	Date of filing of request for examination: 880707
Change:	890614 A2	Representative (change)
*Assignee:	890614 A2	Applicant (transfer of rights) (change): BULL HN Information Systems Inc. (405375) Corporation Trust Center 1209 Orange Street Wilmington County of New Castle Delaware (US) (applicant designated states: BE;CH;DE;FR;GB;IT;LI;NL;SE)
*Assignee:	890614 A2	Previous applicant in case of transfer of rights (change): Honeywell Information Systems Inc. (405371) Honeywell Plaza Minneapolis Minnesota 55408 (US) (applicant designated states: BE;CH;DE;FR;GB;IT;LI;NL;SE)
Examination:	891206 A2	Date of despatch of first examination report: 891023
Withdrawal:	900321 A2	Date on which the European patent application was withdrawn: 900129
*Withdrawal:	900404 A2	Date on which the European patent application was withdrawn (change): 900129

LANGUAGE (Publication,Procedural,Application): English; English; English

3/5/10 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00110037
Operating system supervisor.
Organisationsprogramm fur Betriebssysteme.
Programme superviseur pour systeme d'exploitation.
PATENT ASSIGNEE:
BULL HN Information Systems Inc., (405375), Corporation Trust Center 1209 Orange Street, Wilmington County of New Castle Delaware, (US), (applicant designated states: BE;CH;DE;FR;GB;IT;LI;NL;SE)
INVENTOR:
Angelle, Phillip A., 4615 W. Port au Prince Ln, Glendale Arizona 85306, (US)
Porter, Marion G., 322 W. Encanto Boulevard, Phoenix Arizona, (US)
King, James L. , 1251 W. Rancho Dr, Phoenix Arizona 85013, (US
LEGAL REPRESENTATIVE:
Falcetti, Carlo et al (42243), Bull HN Information Systems Italia S.p.A. Direzione Brevetti, I-20010 Pregnana Milanese (Milano), (IT)
PATENT (CC, No, Kind, Date): EP 106669 A2 840425 (Basic)

EP 106669 A3 870107
EP 106669 B1 900418
APPLICATION (CC, No, Date): EP 83306193 831013;
PRIORITY (CC, No, Date): US 434344 821014
DESIGNATED STATES: BE; CH; DE; FR; GB; IT; LI; NL; SE
INTERNATIONAL PATENT CLASS: **G06F-009/44** ; **G06F-009/46**
CITED PATENTS (EP A): EP 24434 A
CITED REFERENCES (EP A):
COMPCON 1981, DIGEST OF PAPERS VLSI, San Francisco, California, US, 23rd-26th February 1981, pages 229-234, IEEE, New York, US; S. TAKAHASHI et al.: "An "in-line" virtual machine facility";

ABSTRACT EP 106669 A2

Operating system supervisor.

A supervisor, for a data processing system capable of utilizing a plurality of operating system, includes apparatus for identifying a condition in the data processing system requiring a different operating system. A reserved memory area associated with the currently active operating system is then addressed and the **register** contents of a central processing unit are stored in the reserved memory area. The reserved memory of the operating system being activated is addressed and causes the address of the reserved memory of the operating system being activated, the data related to permitting the physical memory associated with the operating system being activated, the contents of **registers** safestored in the reserve-memory, and data establishing the decor of the operating system being activated, all to be entered in the central processing unit. The operating system to be activated is then enabled, and execution of permitted instructions by the second operating system is begun. The physical memory locations are determined by a real address through use of a paging mechanism, permitting storage of portions of the operating system in non-contiguous groups of locations while isolating the memory available to each operating system.

ABSTRACT WORD COUNT: 193

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	840425	A2	Published application (Alwith Search Report ;A2without Search Report)
Change:	850403	A2	Representative (change)
Search Report:	870107	A3	Separate publication of the European or International search report
Examination:	870819	A2	Date of filing of request for examination: 870619
Examination:	880420	A2	Date of despatch of first examination report: 880229
Change:	890816	A2	Representative (change)
*Assignee:	890816	A2	Applicant (transfer of rights) (change): BULL HN Information Systems Inc. (405375) Corporation Trust Center 1209 Orange Street Wilmington County of New Castle Delaware (US) (applicant designated states: BE;CH;DE;FR;GB;IT;LI;NL;SE)
*Assignee:	890816	A2	Previous applicant in case of transfer of rights (change): Honeywell Information Systems Inc. (405370) 200 Smith Street Waltham County of Middlesex, Massachusetts 02154 (US) (applicant designated states: BE;CH;DE;FR;GB;IT;LI;NL;SE)
Grant:	900418	B1	Granted patent
Lapse:	901114	B1	Date of lapse of the European patent in a Contracting State: CH 900418, LI 900418
Lapse:	901212	B1	Date of lapse of the European patent in a Contracting State: CH 900418, LI 900418, SE 900418
Oppn None:	910403	B1	No opposition filed
Lapse:	910424	B1	Date of lapse of the European patent in a Contracting State: CH 900418, LI 900418, NL 900418, SE 900418
Lapse:	910605	B1	Date of lapse of the European patent in a

Contracting State: BE 900418, CH 900418, LI 900418, NL 900418, SE 900418
LANGUAGE (Publication,Procedural,Application): English; English; English

3/5/11 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00110034
Computer system with multiple operating systems.
Rechner mit Mehrfachbetriebssystem.
Ordinateur avec plusieurs systemes d'exploitation.
PATENT ASSIGNEE:
Honeywell Information Systems Inc., 200 Smith Street, Waltham Massachusetts 02154, (US), (applicant designated states: BE;CH;DE;FR;GB;IT;LI;NL;SE)
INVENTOR:
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Wilhite, John Edward, 8225 N. 45th Avenue, Glendale Arizona 85302, (US)
Trubisky, Leonard G., 6725 E. Horseshoe Lane, Scottsdale Arizona 85253, (US)
Angelle, Phillip A., 4615 W. Port au Prince Lane, Glendale Arizona 85306, (US)
Porter, Marion G., 322 W. Encanto Boulevard, Phoenix Arizona, (US
LEGAL REPRESENTATIVE:
Falcetti, Carlo et al (42243), Bull HN Information Systems Italia S.p.A. Direzione Brevetti, I-20010 Pregnana Milanese (Milano), (IT)
PATENT (CC, No, Kind, Date): EP 106668 A2 840425 (Basic)
EP 106668 A3 860416
APPLICATION (CC, No, Date): EP 83306190 831013;
PRIORITY (CC, No, Date): US 434383 821014
DESIGNATED STATES: BE; CH; DE; FR; GB; IT; LI; NL; SE
INTERNATIONAL PATENT CLASS: **G06F-009/44** ; **G06F-009/46**
CITED REFERENCES (EP A):
COMPCON 1981, DIGEST OF PAPERS VLSI, 23th-26th February 1981, pages 229-234, IEEE, New York, US; S. TAKAHASHI et al.: "An "in-line" virtual machine facility"
COMPCON 1981, DIGEST OF PAPERS VLSI, 23th-26th February 1981, pages 229-234, IEEE, New York, US; S. TAKAHASHI et al.: "An "in-line" virtual machine facility";

ABSTRACT EP 106668 A2
Computer system with multiple operating systems.
A supervisor for data processing system capable of utilizing a plurality of operating systems includes apparatus for identifying a condition in the data processing system requiring a different operating system. A reserved memory area associated with the currently active operating system is then addressed and the **register** contents of the central processing unit are stored in the reserved memory area. The reserved memory of the operating system being activated is addressed and causes the address of the reserved memory of the operating system being activated, the data related to permitting the physical memory associated with the operating system being activated, contents of **registers** safestored in the reserve-memory, and data establishing the decor of the operating system being activated all to be entered in the central processing unit. The operating system to be activated is then enabled, and execution of permitted instructions by the second operating system is begun. The physical memory locations are determined by a real address though use of a paging mechanism permitting storage of portions of the operating system in non-contiguous groups of locations while isolating the memory available to each operating system.
ABSTRACT WORD COUNT: 194

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 840425 A2 Published application (A1with Search Report ;A2without Search Report)
Change: 850403 A2 Representative (change)

Search Report:	860416 A3	Separate publication of the European or International search report
Examination:	861120 A2	Date of filing of request for examination: 860920
Examination:	880420 A2	Date of despatch of first examination report: 880308
Change:	890628 A2	Representative (change)
*Assignee:	890628 A2	Applicant (transfer of rights) (change): BULL HN Information Systems Inc. (405375) Corporation Trust Center 1209 Orange Street Wilmington County of New Castle Delaware (US) (applicant designated states: BE;CH;DE;FR;GB;IT;LI;NL;SE)
*Assignee:	890628 A2	Previous applicant in case of transfer of rights (change): Honeywell Information Systems Inc. (405370) 200 Smith Street Waltham County of Middlesex, Massachusetts 02154 (US) (applicant designated states: BE;CH;DE;FR;GB;IT;LI;NL;SE)
Refusal:	900606 A2	Date on which the European patent application was refused: 900120

LANGUAGE (Publication,Procedural,Application): English; English; English

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File 275:Gale Group Computer DB(TM) 1983-2003/Jul 30
         (c) 2003 The Gale Group
File 621:Gale Group New Prod.Annou.(R) 1985-2003/Jul 30
         (c) 2003 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2003/Jul 30
         (c) 2003 The Gale Group
File  16:Gale Group PROMT(R) 1990-2003/Jul 30
         (c) 2003 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 148:Gale Group Trade & Industry DB 1976-2003/Jul 30
         (c)2003 The Gale Group
File 624:McGraw-Hill Publications 1985-2003/Jul 29
         (c) 2003 McGraw-Hill Co. Inc
File  15:ABI/Inform(R) 1971-2003/Jul 30
         (c) 2003 ProQuest Info&Learning
File 647:CMP  Computer Fulltext 1988-2003/Jul W1
         (c) 2003 CMP Media, LLC
File 674:Computer News Fulltext 1989-2003/Jul W3
         (c) 2003 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2003/Jul 30
         (c) 2003 The Dialog Corp.
File 369:New Scientist 1994-2003/Jul W3
         (c) 2003 Reed Business Information Ltd.

Set      Items   Description
S1      434884   REGISTER? ?
S2       32492   S1(5N)(ACCESS??? OR READ??? OR SCAN???? OR RETRIEV??? OR O-
             BTAIN??? OR GET???? OR POLL??? OR CHECK??? OR EXAMIN? OR ACQU-
             IR??? OR ACQUISITION OR TAP???? OR WRIT??? OR MANIPULAT? OR C-
             ONFIGUR? OR FETCH???)
S3      716537   (GRAPHIC? OR WINDOW?)(2W)INTERFACE? ? OR GUI OR GUIS OR BR-
             OWSER? ? OR GRAPHIC??(2W)(SCREEN? ? OR DISPLAY? ? OR PANE?? OR
              MONITOR? ? OR PROGRAM? OR APPLICATION? ? OR SOFTWARE)
S4      293183   CAD OR CAM OR CAE OR COMPUTER()(ASSISTED OR AIDED)()(DRAWI-
             NG OR DESIGN? OR MANUFACTUR??? OR ENGINEERING)
S5       40523   DEVICE? ?(5N)DRIVER? ?
S6         576   S2(S)S3:S4
S7       25396   S1(5N)(DEVICE? ? OR PERIPHERAL? ? OR HARDWARE? ? OR MACHIN-
             E? ? OR UNIT? ? OR PROCESSOR? ? OR COMPUTER? ? OR PC? ? OR IN-
             STRUMENT? ? OR SETTOP OR BOX?? OR MODULE? ? OR EQUIPMENT? ? OR
              TERMINAL? ? OR CLIENT? ? OR WORKSTATION? ?)
S8        2954   S1(5N)(WORK()STATION? ? OR PRINTER? ? OR COPIER? ? OR SCAN-
             NER? ? OR MONITOR? ?)
S9          84   S2(S)S3:S4(S)S7:S8
S10         51   RD (unique items)
S11         42   S10 NOT PD>20001220
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File 348:EUROPEAN PATENTS 1978-2003/Jul W03
(c) 2003 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20030724,UT=20030717
(c) 2003 WIPO/Univentio

Set	Items	Description
S1	90584	REGISTER? ?
S2	25588	S1(5N)(ACCESS??? OR READ??? OR SCAN???? OR RETRIEV??? OR OBTAIN??? OR GET???? OR POLL??? OR CHECK??? OR EXAMIN? OR ACQUIR??? OR ACQUISITION OR TAP???? OR WRIT??? OR MANIPULAT? OR CONFIGUR? OR FETCH???)
S3	41391	(GRAPHIC? OR WINDOW?)(2W)INTERFACE? ? OR GUI OR GUIS OR BROWSER? ? OR GRAPHIC??(2W)(SCREEN? ? OR DISPLAY? ? OR PANE?? OR MONITOR? ? OR PROGRAM???? OR APPLICATION? ? OR SOFTWARE)
S4	62230	CAD OR CAM OR CAE OR COMPUTER()(ASSISTED OR AIDED)()(DRAWING OR DESIGN? OR MANUFACTUR??? OR ENGINEERING)
S5	11736	DEVICE? ?(5N)DRIVER? ?
S6	543	S2(S)S3:S4
S7	99	S6/TI,AB,CM
S8	14	S7 AND IC=G09G
S9	50	S7 AND IC=G06F
S10	47	S9 NOT S8
S11	38	S7 NOT (S8 OR S10)
S12	5713	S2/TI,AB,CM
S13	173	S12 AND S6
S14	74	S13 NOT S7

10/5,K/6 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00946931 **Image available**
COMPUTER - AIDED DESIGN **SYSTEM TO AUTOMATE** SCAN **SYNTHESIS AT** REGISTER **-TRANSFER LEVEL**
SYSTEME DE CONCEPTION ASSISTE PAR ORDINATEUR POUR AUTOMATISER LA SYNTHESE DE BALAYAGE AU NIVEAU DU TRANSFERT DE REGISTRE

Patent Applicant/Assignee:
SYNTEST TECHNOLOGIES INC, 505 S. Pastoria Avenue, Suite 101, Sunnyvale, CA 94086, US, US (Residence), US (Nationality)
Patent Applicant/Inventor:
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LIN Shyh-Horng, 3F., No. 3, Lane 289, Section 2, Li-Nong St., Taipei 112, TW, -- (Residence), -- (Nationality), (Designated only for: US)
WANG Hsin-Po, No. 4, Alley 1, Lane 122, Section 2, Chung-Hsin Road, Chu-Tung, Hsinchu 310, TW, -- (Residence), -- (Nationality), (Designated only for: US)
WEN Xiaoqing, 705 W. Fremont Ave., #4, Sunnyvale, CA 94087-2304, US, -- (Residence), -- (Nationality), (Designated only for: US)
KILFI Augusli, No. 166, Lane 271, Wuling Rd., Hsinchu 300, TW, -- (Residence), -- (Nationality), (Designated only for: US)
HSU Fei-Sheng, No. 20, Alley 16, Lane 85, Fyuchu St., Hsinchu 300, TW, -- (Residence), -- (Nationality), (Designated only for: US)
Legal Representative:
ZEGEER Jim (agent), 801 North Pitt Street, #108, Alexandria, VA 22314, US

Patent and Priority Information (Country, Number, Date):
Patent: WO 200280046 A2-A3 20021010 (WO 0280046)
Application: WO 2002US6671 20020329 (PCT/WO US0206671)
Priority Application: US 2001279710 20010330; US 2002108238 20020328
Designated States: AU CA CN IN JP NZ US
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
Main International Patent Class: **G06F-017/50**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 21341

English Abstract
A method and system to automate scan synthesis at register-transfer level "RTL". The method and system will produce scan HDL code(215) modeled at RTL for an integrated circuit modeled at RTL. The method and system comprise computer-implemented steps of performing RTL testability point selection(208) , scan repair and test point insertion(209), scan replacement and scan stitching(210), scan extraction(211), interactive scan debug(212), interactive scan repair(213), and flush/random test bench generation(214). In addition, the present invention further comprises a method and system for hierarchical scan synthesis by performing scan synthesis module-by-module and then stitching these scanned modules together at top-level(2309). The present invention further comprises integrating and verifying the scan HDL code with other design-for-test "DFT" HDL code, including boundary-scan and logic BIST "built-in self-test"(2503).

French Abstract
L'invention concerne un procede et un systeme permettant d'automatiser la synthese de balayage au niveau du transfert de registre "RTL". Le procede et le systeme permettront de produire un code HDL (215) de balayage modelise au RTL pour un circuit integre modelise au RTL. Le procede et le systeme comportent des etapes mises en oeuvre par ordinateur, qui consistent a effectuer une selection de point de testabilite (208) RTL,

une reparation par balayage et une insertion de point de test (209), un remplacement par balayage et un maillage par balayage (210), une extraction par balayage (211), une mise au point par balayage interactif (212), une reparation par balayage interactif (213), et une production de banc d'essais de vidage/au hasard (214). En outre, l'invention concerne un procede et un systeme de synthese de balayage hierarchique permettant de realiser une synthese de balayage module par module et ensuite de mailler ensemble ces modules balayes au niveau superieur (2309). L'invention concerne egalement l'integration et la verification du code HDL de balayage par rapport a un autre code HDL de testabilite, y compris le balayage des limites et l'autoverification integree logique (BIST) (2503).

Legal Status (Type, Date, Text)
Publication 20021010 A2 Without international search report and to be republished upon receipt of that report.
Search Rpt 20021212 Late publication of international search report
Republication 20021212 A3 With international search report.
Examination 20030116 Request for preliminary examination prior to end of 19th month from priority date

COMPUTER - AIDED DESIGN **SYSTEM TO AUTOMATE** SCAN **SYNTHESIS AT** REGISTER **-TRANSFER LEVEL**
Main International Patent Class: **G06F-017/50**

10/5,K/8 (Item 3 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00908922 **Image available**
MULTIPLE DEVICE SCAN CHAIN EMULATION/DEBUGGING
EMULATION/DEBOGAGE DANS UNE CHAINE DE REGISTRE AVEC DE MULTIPLES DISPOSITIFS
Patent Applicant/Assignee:
WIND RIVER SYSTEMS INC, 500 Wind River Way, Alameda, CA 94501, US, US (Residence), US (Nationality)
Inventor(s):
O'BRIEN James J, 4 Town Way, Hull, MA 02045, US,
Legal Representative:
SAMPSON Richard L (agent), Sampson & Associates, P.C., 50 Congress Street, Boston, MA 02109, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200242949 A1 20020530 (WO 0242949)
Application: WO 2001US48003 20011116 (PCT/WO US0148003)
Priority Application: US 2000252316 20001121; US 2001921250 20010802
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-017/50**
International Patent Class: **G06F-011/00**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 7583

English Abstract
A method and system is provided for emulating individual JTAG devices in a multiple device boundary scan chain (Figure 7B). The method includes coupling an emulator to the scan chain (170), and obtaining the topology of the scan chain (172). One device within the scan chain is then

selected, and at least one other device within the scan chain is placed into bypass mode (182). Emulation instructions are sent to the scan chain, (188) so that the emulation instructions bypass the at least one other device and are executed by the one device.

French Abstract

L'invention concerne un procede et un systeme permettant l'emulation de dispositifs individuels JTAG dans une chaine de registre (Figure 7B) a decalage peripherique de multiples dispositifs. Le procede consiste a coupler un emulateur a la chaine de registre (170) et a obtenir la topologie de ladite chaine (172). On selectionne ensuite un des dispositifs et on place au moins un autre dispositif en mode derivation (182). Les instructions d'emulation sont envoyees a la chaine de registre (188) de telle sorte que les instructions contournent au moins le dispositif en question et soient executees par ce meme dispositif.

Legal Status (Type, Date, Text)
Publication 20020530 A1 With international search report.
Publication 20020530 A1 Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

Main International Patent Class: **G06F-017/50**
International Patent Class: **G06F-011/00**
Fulltext Availability:
Claims
Claim
... field displays a parameter selected from the group consisting of. number of devices in the **scan** chain; number of instruction **register** bits in the **scan** chain; and a device number for at least one of the devices.

26 The GUI...

10/5,K/15 (Item 10 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00844274 **Image available**
WEB SITE ADDRESS AUTOMATIC MATCH SYSTEM USING REMOTE-CONTROLLER HAVING A OPTICAL SCANNER AND METHOD THEREOF
SYSTEME DE CONCORDANCE AUTOMATIQUE D'ADRESSES DE SITES WEB UTILISANT UNE TELECOMMANDE POURVUE D'UN SCANNER NUMERIQUE ET PROCEDE ASSOCIE
Patent Applicant/Assignee:
INTERNET TV SOC CO LTD, Representation: Kim, Jong, Hyun, Genoa Building, 7th Floor, 839-13, Yeoksam-Dong, Kangnam-Gu, Seoul 135-080, KR, KR (Residence), KR (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
HAN Jong Suk, 3948, Shingil-Dong, Youngdungpo-Gu, Seoul 150-050, KR, KR (Residence), KR (Nationality), (Designated only for: US)
Legal Representative:
KIM Tae Gon (agent), Hansun International Patent & Law Office, #202 New Seoul Building, Yeoksam-Dong, Kangnam-Gu, Seoul 135-080, KR,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200177865 A1 20011018 (WO 0177865)
Application: WO 2000KR833 20000731 (PCT/WO KR0000833)
Priority Application: KR 200018412 20000408
Designated States: DE JP US
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: **G06F-017/00**
Publication Language: English
Filing Language: Korean
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 5407

English Abstract

An Internet site accessing system and method wherein a coupled version of a remote controller and an optical scanner is provided to read a Web address on a given paper and transmit information about the read Web address by radio. The system comprises a scan remote control device (10) for reading a Web address on a given paper and processing the read Web address to generate and transmit an infrared-ray data stream for remote control, and a set-top box (20) for receiving the infrared-ray data stream from the device (10), determining whether the read Web address corresponds to a previously registered sponsor company and, if the read Web address corresponds to the previously registered sponsor company, generating the real Web address in a uniform resource locator box of a Web browser and automatically executing an Internet connection to a site of the read Web address.

French Abstract

L'invention concerne un systeme et un procede d'acces a des sites Internet. Une version couplee de telecommande et de scanner numerique permet de lire une adresse web sur un document donne et de la communiquer par radio. Le systeme comporte un dispositif (10) de telecommande a balayage qui lit une adresse web sur un document donne et la traite pour creer et communiquer un train de donnees a rayons infrarouges pour telecommande, ainsi qu'un decodeur (20) qui recoit, du dispositif (10), le train de donnees a rayons infrarouges, determine si l'adresse web lue correspond a une entreprise commanditaire deja enregistree et, si tel est le cas, cree l'adresse web lue dans la case localisateur de ressources universel d'un navigateur web et execute automatiquement une liaison Internet vers un site de ladite adresse.

Legal Status (Type, Date, Text)
Publication 20011018 A1 With international search report.

Main International Patent Class: **G06F-017/00**
Fulltext Availability:
Claims
Claim
... allowing a set-top box to receive said infrared-ray data stream transmitted from said **scan** remote control device, **register** said **read** Web address in a uniform resource locator box of a Web **browser** and run said **browser** .

8 The Internet site accessing method as set forth in Claim 7, farther comprising the...

10/5,K/16 (Item 11 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00837831 **Image available**
ELECTRONIC COMMERCE AND INFORMATION CONTROL SYSTEM
SYSTEME ET PROCEDES DE COMMERCE ELECTRONIQUE PRESENTANT DES INFORMATIONS GLOBALES ACCESSIBLES ET DES INFORMATIONS ET CONTROLES SPECIFIQUES DISPONIBLES
Patent Applicant/Assignee:
FOUND INC, Suite 200, 6671 South Redwood Road, Salt Lake City, UT 84084, US, US (Residence), -- (Nationality)
Patent Applicant/Inventor:
LAWSON Richard, Suite 400, 200 Pine Street, San Francisco, CA 94104, US, US (Residence), US (Nationality)
DRIES Gene, 10024 Pourdre Court, Littleton, CO 80124, US, US (Residence), US (Nationality)
Legal Representative:
O'BRYANT David W (agent), Morris, Bateman, O'Bryant & Compagni, P.C., 136 South Main Street, Suite 700, Salt Lake City, UT 84101, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200171456 A2-A3 20010927 (WO 0171456)
Application: WO 2001US8810 20010320 (PCT/WO US0108810)
Priority Application: US 2000528504 20000320

Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU
CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR
KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE
SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-017/60**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 9905

English Abstract
ABSTRACT Systems and methods are disclosed for facilitating electronic commerce over a global communications network. A method of providing electronic commerce over a global communications network (28) includes the step of browsing a first web site (158) where the first web site is offering items for sale. The first web site is operated by a first company that also is affiliated with a physical store (160). The method includes the step of a consumer or user selecting an option to shop the physical store (160) via the global communications network (28). In addition, the method includes the step of offering a certain item at the physical store (160) for the certain item requested. The method for providing electronic commerce also includes the step of offering to the user, by the server system, the ability to purchase the certain item from the physical store (160). The method further includes the step of communicating to the physical store (160) information describing the certain item. The information may include the method of payment and means of fulfillment.

French Abstract
L'invention concerne des systemes et des procedes qui servent a faciliter le commerce electronique dans un reseau universel de telecommunications. Un procede de mise en oeuvre d'un commerce electronique dans un reseau universel de telecommunications consiste a naviguer dans un premier site web offrant des articles a vendre. Ce premier site web est gere par une premiere entreprise egalement partenaire d'un magasin physique. Un consommateur ou un utilisateur choisit une option lui permettant d'effectuer des achats au magasin physique par l'intermediaire du reseau universel de telecommunications. Le procede consiste a offrir a l'utilisateur, par le biais d'un systeme serveur, la possibilite de chercher si un certain article est disponible au magasin physique. Le systeme serveur interroge ensuite une base de donnees d'articles disponibles au magasin physique a la recherche de l'article. Le procede de commerce electronique consiste ensuite a offrir a l'utilisateur, par le biais du systeme serveur, la possibilite d'acheter ledit article au magasin physique. Le procede consiste enfin a communiquer au magasin physique une information decrivant ledit article, laquelle information pouvant inclure un mode de paiement et des moyens d'execution.

Legal Status (Type, Date, Text)

Publication	20010927	A2 Without international search report and to be republished upon receipt of that report.
Search Rpt	20020404	Late publication of international search report
Republication	20020404	A3 With international search report.
Examination	20020510	Request for preliminary examination prior to end of 19th month from priority date

Main International Patent Class: **G06F-017/60**
Fulltext Availability:
Claims

Claim
... data 84. etc. 25 In an embodiment, the client software 76 may be a web

browser . such as Microsoft's Internet Explorer or Netscape Navigator. As known in the art, these **browsers** can use and call libraries 80 and plug-ins 82. In addition, a **browser** accesses configuration 78 to configure itself for the particular user. In addition. the **browser** may store history data 84 to indicate where the user has been on the Internet ...soft%vare for Input processing 98 to tile store computers 24. For example. typical cash **registers** Include an interface for a **scanner** for scanning items being sold. A similar scanner may be used with the store 25...

10/5,K/37 (Item 32 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00543724 **Image available**
PROCESSOR CONFIGURED TO SELECTIVELY FREE PHYSICAL REGISTERS UPON RETIREMENT OF INSTRUCTIONS
PROCESSEUR CONFIGURE POUR LIBERER SELECTIVEMENT DES REGISTRES PHYSIQUES SUR RETRAIT D'INSTRUCTIONS
Patent Applicant/Assignee:
ADVANCED MICRO DEVICES INC,
Inventor(s):
WITT David B,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200007097 A1 20000210 (WO 0007097)
Application: WO 99US1048 19990118 (PCT/WO US9901048)
Priority Application: US 98127094 19980731
Designated States: JP KR AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: **G06F-009/38**
International Patent Class: **G06F-009/30**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 20043

English Abstract
A processor employing a map unit including register renaming hardware is shown. The map unit may assign virtual **register** numbers to source **registers** by **scanning** instruction operations to detect intraline dependencies. Subsequently, physical register numbers are mapped to the source register numbers responsive to the virtual register numbers. The map unit may store (e.g. in a map silo) a current lookahead state corresponding to each line of instruction operations which are processed by the map unit. Additionally, the map unit stores an indication of which instruction operations within the line update logical registers, which logical registers are updated, and the physical register numbers assigned to the instruction operations. Upon detection of an exception condition for an instruction operation with a line, the current look a head state corresponding to the line is restored from the map silo. Additionally, physical register numbers corresponding to instruction operations within the line which are prior to the instruction operation experiencing the exception are restored into the current lookahead state. The map unit may use the same physical register to store both a condition code result and an integer result. The physical register number identifying the physical register is recorded for both the condition code register and the integer register. The map unit pops the previous renames from the architected renames block upon retiring one or more instruction operations. The popped physical register numbers are cammed against the updated architectural state. If a **cam** match is detected, the popped physical register is not freed.

French Abstract
L'invention concerne un processeur utilisant une unite de correspondance comprenant un materiel de renommage de registres. L'unite de correspondance peut attribuer des nombres de registres virtuels a des

registres sources pa[redacted] operations d'instruction par balayage en vue de detecter des dependances d'intra-lignes. Les nombres de registres physiques sont ensuite mis en correspondance avec les nombres de registres sources repondant aux nombres de registres virtuels. L'unite de correspondance peut memoriser (par exemple, dans un silo de correspondance) un etat anticipe courant correspondant a chaque ligne d'operations d'instruction traitees par ladite unite de correspondance. En outre, l'unite de correspondance memorise une indication selectionnant des operations d'instruction dans la ligne des registres logiques de mise a jour, lesquels registres sont mis a jour et les nombres de registres physiques sont attribues aux operations d'instructions. Apres detection d'une condition d'exception pour une operation d'instruction avec une ligne, l'etat anticipe courant correspondant a la ligne est restaure par le silo de correspondance. En outre, des nombres de registres physiques correspondant aux operations d'instructions dans la ligne anterieure a l'operation d'instruction rencontrant l'exception sont restaures en l'etat anticipe courant. L'unite de correspondance peut utiliser le meme registre physique pour memoriser a la fois un resultat de code de condition et un resultat entier. Le nombre de registres physiques identifiant le registre physique est enregistre a la fois pour le registre de code de condition et le registre entier. L'unite de correspondance fait sortir le renommage anterieur du bloc de renommage structure en retirant une ou plusieurs operations d'instruction. Les nombres de registres physiques sortis sont compares a l'etat structure mis a jour. Si une correspondance est detectee, le registre physique sorti n'est pas libere.

Main International Patent Class: **G06F-009/38**
International Patent Class: **G06F-009/30**
Fulltext Availability:
Claims

English Abstract
...a map unit including register renaming hardware is shown. The map unit may assign virtual **register** numbers to source **registers** by **scanning** instruction operations to detect intraline dependencies. Subsequently, physical register numbers are mapped to the source...

...operations. The popped physical register numbers are cammed against the updated architectural state. If a **cam** match is detected, the popped physical register is not freed.

Claim
... Dest Reg Dest Reg
- 60B 92 Q Tail
Numbers Numbers IF ointers
ROP
Alloc 11
Register **Scan** Unit IQ #/PR# Control Unit
1 82
Ass.
est Reg Src Virtual Register
Numbers Numbers...

...I Register Register Map Unit PR#
32 State r 72
84 86
64 Free List **Cam**
Src/Dest PR# and IQ
Control Unit Matches
74
8
Free
Free List
F 94...unit 82)
Virtual Next
Lookahead
Virtual Src

Virtual Src Reg Sta (from Reg
Numbers (from **register** **scan** Numbers
register sca unit 80)
(from
unit 80)
76A **register**
Recovery **scan** unit
Trap (from PC IF A
Virtual/Physical I Trap (from P
Register Map Unit...
...84 36A-3613 F
FIG. 8
/10
R# (Line Portion)
Valid ROPs within Line
ROP **Register** **Writes**
Assigned PR#
Assigned IQ#
Logical **Register** Numbers
CC **Writes**
Current Lookahead **Register** State
FP TOS and Valid Bits (Each Issue Position)
1 8 FIG. 9
184 /- 1186 188
V IQ# PR#
182 FIG. 10
/10
ta
Cam R# Against Mapper
Silo, Cancel More Recent F190
Entries (and Free Allocated
PR#)
Restore Lookahead...

...Silo Entry
Restore FP TOS and Valid F194
Bits to Correspond to
Exception Instruction
Mask **Register** **Writes** to
Those Prior to Exception 196
Instruction, Scan for Most F
Recent **Writes** to Each
Register , and Update
Current Lookahead State
Mask **Register** **Writes** to 198
Those Subsequent to F
Exception Instruction, Free
PR#
FIG, 1 1
Main Memory...

10/5,K/38 (Item 33 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00543723 **Image available**
PROCESSOR CONFIGURED TO MAP LOGICAL REGISTER NUMBERS TO PHYSICAL REGISTER NUMBERS USING VIRTUAL REGISTER NUMBERS
PROCESSEUR CONFIGURE POUR ETABLIR UNE CORRESPONDANCE ENTRE DES NOMBRES DE REGISTRES LOGIQUES ET DES NOMBRES DE REGISTRES PHYSIQUES A L'AIDE DE NOMBRES DE REGISTRES VIRTUELS
Patent Applicant/Assignee:
ADVANCED MICRO DEVICES INC,
Inventor(s):
WITT David B,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200007096 A1 20000210 (WO 0007096)

Application: WO 99US1046 19990118 (PCT/WO 9901046)
Priority Application: US 98127100 19980731
Designated States: JP KR AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: **G06F-009/38**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 19339

English Abstract
A processor employing a map unit including register renaming hardware is shown. The map unit may assign virtual **register** numbers to source **registers** by **scanning** instruction operations to detect intraline dependencies. Subsequently, physical register numbers are mapped to the source register numbers responsive to the virtual register numbers. The map unit may store (e.g. in a map silo) a current lookahead state corresponding to each line of instruction operations which are processed by the map unit. Additionally, the map unit stores an indication of which instruction operations within the line update logical registers, which logical registers are updated, and the physical register numbers assigned to the instruction operations. Upon detection of an exception condition for an instruction operation with a line, the current lookahead state corresponding to the line is restored from the map silo. Additionally, physical register numbers corresponding to instruction operations within the line which are prior to the instruction operation experiencing the exception are restored into the current lookahead state. The map unit may use the same physical register to store both a condition code result and an integer result. The physical register number identifying the physical register is recorded for both the condition code register and the integer register. The map unit pops the previous renames from the architected renames block upon retiring one or more instruction operations. The popped physical register numbers are cammed against the updated architectural state. If a **cam** match is detected, the popped physical register is not freed.

French Abstract
L'invention concerne un processeur utilisant une unite de correspondance comprenant un materiel de renommage de registres. L'unite de correspondance peut attribuer des nombres de registres virtuels a des registres sources par operations d'instruction par balayage en vue de detecter des dependances d'intra-lignes. Les nombres de registres physiques sont ensuite mis en correspondance avec les nombres de registres sources repondant aux nombres de registres virtuels. L'unite de correspondance peut memoriser (par exemple, dans un silo de correspondance) un etat anticipe courant correspondant a chaque ligne d'operations d'instruction traitees par ladite unite de correspondance. En outre, l'unite de corrrespondance memorise une indication selectionnant des operations d'instruction dans la ligne des registres logiques de mise a jour, lesquels registres sont mis a jour et les nombres de registres physiques sont attribues aux operations d'instructions. Apres detection d'une condition d'exception pour une operation d'instruction avec une ligne, l'etat anticipe courant correspondant a la ligne est restaure par le silo de correspondance. En outre, des nombres de registres physiques correspondant aux operations d'instructions dans la ligne anterieure a l'operation d'instruction rencontrant l'exception sont restaures en l'etat anticipe courant. L'unite de correspondance peut utiliser le meme registre physique pour memoriser a la fois un resultat de code de condition et un resultat entier. Le nombre de registres physiques identifiant le registre physique est enregistre a la fois pour le registre de code de condition et le registre entier. L'unite de correspondance fait sortir le renommage anterieur du bloc de renommage structure en retirant une ou plusieurs operations d'instruction. Les nombres de registres physiques sortis sont compares a l'etat structure mis a jour. Si une correspondance est detectee, le registre physique sorti n'est pas libere.

Main International Patent Class: **G06F-009/38**
Fulltext Availability:
Claims

English Abstract
...a map unit including register renaming hardware is shown. The map unit may assign virtual **register** numbers to source **registers** by **scanning** instruction operations to detect intraline dependencies. Subsequently, physical register numbers are mapped to the source...

...operations. The popped physical register numbers are cammed against the updated architectural state. If a **cam** match is detected, the popped physical register is not freed.

Claim
... source register number within said plurality of source register numbers, and wherein said processor is **configured** to map said particular physical **register** number to said particular source register number responsive to said particular virtual register number.
3...

...Regs, 68 Silo 48
Prev. PR# PR#
70 Exception
72 Valid, R#
75
from PC
Cam Silo 48
Matches Architectural Renames
74 Block
34
FIG. 2
from Decode Unit from Decode...

...Dest Reg Dest Reg Q Tail
60A 6(bi
Numbers Numbers 1B ointers
ROP
Alloc
Register **Scan** Unit IQ #/PR# Control Unit
80 82
Dest Reg Src Virtual Register Ass.
Numbers Numbers...

...Physical PR# PR#
Silo Register Map Unit 72
32 State 84] 86
64 Free List **Cam**
Src/Dest PR# and IQ
Control Unit Matches R
88 74
J
78
Free
Free...Virtual Next unit 82)
Lookahead Virtual Src
Virtual Src Reg State (from Reg
Numbers (from **register** **scan**
2 Numbers
register **scan** unit 80)
(from
unit 80)
76A **register**
Recovery **scan** unit
Trap (from PC Trap (from PC
Virtual/Physical Silo 48) ookahead 80) Silo 48...

...84 36A-36B Re(

FIG. 8
/10
R# (Line Portion)
Valid ROPs within Line
ROP **Register** **Writes**
Assigned PR#
Assigned IQ#
Logical **Register** Numbers
CC **Writes**
Current Lookahead **Register** State
FP TOS and Valid Bits (Each Issue Position)
180 FIG. 9
184 /- 186 188
IQ# PR#
182 FIG. 1 0
/10
ta
Cam R# Against Mapper 190
Silo, Cancel More RecentF
Entries (and Free Allocated
PR#)
Restore Lookahead...

...Silo Entry
Restore FP TOS and Valid 194
Bits to Correspond to
Exception Instruction
Mask **Register** **Writes** to
Those Prior to Exception 196
Instruction, Scan for Most
Recent **Writes** to Each
Register , and Update
Current Lookahead State
Mask **Register** **Writes** to 198
Those Subsequent to F
Exception Instruction, Free
PR#
FIG. 1 1
Main Memory...

10/5,K/39 (Item 34 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00539943 **Image available**
A METHOD FOR SECURING ACCESS TO A REMOTE SYSTEM
PROCEDE POUR SECURISER L'ACCES A UN SYSTEME DISTANT
Patent Applicant/Assignee:
TELEFONAKTIEBOLAGET LM ERICSSON (publ),
Inventor(s):
RATAYCZAK Georg,
NIEBERT Norbert,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200003316 A1 20000120 (WO 0003316)
Application: WO 98EP4249 19980708 (PCT/WO EP9804249)
Priority Application: WO 98EP4249 19980708
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES
FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD
MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ
VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH
CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW
ML MR NE SN TD TG
Main International Patent Class: **G06F-001/00**
International Patent Class: H04L-029/06
Publication Language: English
Fulltext Availability:
Detailed Description

Claims
Fulltext Word Count: 5477

English Abstract
Method for secure user access to a remote system using a communications device. Access to the system is released only after the input of valid code words via independent communications devices. One of the communications devices may be a data processing unit and the second communications device may be a mobile telephone.

French Abstract
L'invention concerne un procede pour securiser l'acces des utilisateurs a un systeme distant au moyen d'un dispositif de communication. L'acces au systeme est permis uniquement apres l'introduction de mots de code valables au moyen de dispositifs de communication independants. Un des dispositifs de communication peut se presenter comme une unite de traitement de donnees, l'autre dispositif de communication pouvant etre un telephone mobile.

Main International Patent Class: **G06F-001/00**
Fulltext Availability:
Claims

Claim
... of the Internet. In this embodiment, access is advantageously controlled to the HLR (home location **register**) by the **access** device A. In thie HLR **register** , subscriber-specific data are stored, for example for services such as forwarding of calls or...access device, access to system S can be obtained. In the embodiment, supported by a **graphic display** of the data processing unit E2, the subscriber-specific user profile in an HLR of...

10/5,K/40 (Item 35 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00527716 **Image available**
METHOD AND APPARATUS FOR PROGRAMMING A GRAPHICS SUBSYSTEM REGISTER SET
PROCEDE ET APPAREIL POUR PROGRAMMER UN ENSEMBLE DE REGISTRES DANS UN PROCESSEUR GRAPHIQUE
Patent Applicant/Assignee:
S3 INCORPORATED,
Inventor(s):
LARSON Michael K,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9959068 A1 19991118
Application: WO 98US9688 19980512 (PCT/WO US9809688)
Priority Application: WO 98US9688 19980512
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Main International Patent Class: **G06F-012/06**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 5361

English Abstract
A graphics system (Figure 3) includes a graphics processor (310) for rendering graphics primitives with a display list. A host processor (302) generates a display list which includes a command format for loading the display list into a register file (312). The graphics processor (310)

includes logic (410) to encode and decode the command register to sequentially load the display list into the register file (312) without a physical reference to the register being loaded. The command register may also be programmed to allow the gaphics processor (310) to randomly load register file (312) thereby shortening the processing of the display list and allowing the display list to be written during a burst cycle mode of bus operation.

French Abstract

L'invention concerne un systeme graphique (figure 3) qui comprend un processeur graphique (310) pour le rendu de primitives graphiques avec une liste d'affichage. Un processeur central (302) genere une liste d'affichage qui comprend un format de commande pour le chargement de la liste d'affichage dans une pile de registres (312). Le processeur graphique (310) comprend un circuit logique (410) pour coder et decoder le registre de commandes, afin de charger sequentiellement la liste d'affichage dans la pile de registres (312) sans qu'une reference physique au registre soit chargee. Le registre de commandes peut egalement etre programme pour permettre au processeur graphique (310) de charger de facon aleatoire la pile de registres (312), ce qui raccourcit le traitement de la liste d'affichage et permet a celle-ci d'etre ecrite au cours du fonctionnement du bus selon le mode par cycles de salves.

Main International Patent Class: **G06F-012/06**
Fulltext Availability:
Claims

Claim
... through a sequential address range without absolute address referencing to each register.
24

12 A **graphics** processor for **programming** graphics primitives addresses to perform burst write cycle operations, comprising:
an address generator disposed within...a host system memory address range to allow the graphics processor to
10 generate burst **write** cycle to program **registers** in a register file;
11 and
programming logic for programming the registers in the
13...

10/5,K/41 (Item 36 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00478146 **Image available**
SYSTEM AND METHOD FOR CONVERTING GRAPHICAL PROGRAMS INTO HARDWARE IMPLEMENTATIONS
CONVERSION DE PROGRAMMES GRAPHIQUES EN REALISATIONS MATERIELLES ET SYSTEME CORRESPONDANT
Patent Applicant/Assignee:
NATIONAL INSTRUMENTS CORPORATION,
Inventor(s):
KODOSKY Jeffrey L,
ANDRADE Hugo,
ODOM Brian K,
BUTLER Cary P,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9909498 A1 19990225
Application: WO 98US13040 19980622 (PCT/WO US9813040)
Priority Application: US 97912427 19970818
Designated States: CA JP AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: **G06F-017/50**
Publication Language: English
Fulltext Availability:

Detailed Description
Claims
Fulltext Word Count: 21796

English Abstract
A computer-implemented system and method for generating a hardware implementation of graphical code. The method comprises first creating a graphical program. A first portion of the graphical program may optionally be compiled into machine code for execution by a CPU. A second portion of the graphical program is converted into a hardware implementation according to the present invention. The opertion of converting the graphical program into a hardware implementation comprises exporting the second portion of the graphical program into a hardware description, wherein the hardware description describes a hardware implementation of the second portion of the graphical program, and then configuring a programmable hardware element utilizing the hardware description to produce a configured hardware element. The configured hardware element thus implements a hardware implementation of the second portion of the graphical program.

French Abstract
La presente invention concerne un systeme et un procede informatique de generation de mise en oeuvre materielle de code graphique. Le procede consiste d'abord a creer un programme graphique. Une premiere partie du programme graphique peut eventuellement etre compilee en code machine pour execution par une UC. Une deuxieme partie du programme graphique est convertie en mise en oeuvre materielle conformement a la presente invention. L'operation de conversion du programme graphique en mise en oeuvre materielle consiste a exporter la deuxieme partie du programme graphique en une description materielle, laquelle description materielle decrit une mise en oeuvre materielle de la deuxieme partie du programme graphique. Le procede consiste ensuite a configurer un element materiel programmable en utilisant la description materielle afin de produire un element materiel configure. L'element materiel ainsi configure represente une mise en oeuvre materielle de la deuxieme partie du programme graphique.

Main International Patent Class: **G06F-017/50**
Fulltext Availability:
Claims

Claim
... which provide inputs to the respective node.
9 The method of claim 7, wherein the **graphical program** includes an input terminal;
wherein, for said input terminal, said converting comprises:
determining if data...

...supervisory portion executing on the computer system;
I 0 creating a hardware description of a **write register** , wherein the **write register** includes one or more data outputs and at least control output.

10 The method of...of the node to said AND gate.

14 The method of claim 7, wherein the **graphical program** includes an output terminal;
wherein, for said output terminal, said converting comprises:
deten-nining if...

...to a supervisory portion executing on the computer system;
creating a hardware description of a **read register** , wherein the **read register** includes one or more 1 5 data inputs and at least control input.

15 The...

10/5,K/44 (Item 39 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00211830
COMPUTER WITH TABLET INPUT TO STANDARD PROGRAMS
ORDINATEUR COMPRENANT UNE ENTREE PAR NUMERISEUR POUR DES PROGRAMMES STANDARD

Patent Applicant/Assignee:
WANG LABORATORIES INC,
Inventor(s):
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HUNTINGTON Jonathan T II,
MCNALLY J Michael,
BARRETT David M,
WARD Jean Renard,

Patent and Priority Information (Country, Number, Date):
Patent: WO 9209037 A1 19920529
Application: WO 91US4460 19910620 (PCT/WO US9104460)
Priority Application: US 90324 19901113
Designated States: AT AU BE CA CH DE DK ES FR GB GR IT JP LU NL SE
Main International Patent Class: **G06F-015/02**
International Patent Class: **G06F-03:033**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 21971

English Abstract
A computer system having a digitizing tablet overlaying the display screen. The tablet serves as a user's primary input device. Various features of the system make it possible for the user to run and interact with standard programs designed for keystroke and mouse input and not designed for use with a tablet. In addition to the main processor, on which the user's programs are executed, there is an interface processor. In addition to a standard display buffer, there is an ink plane buffer for interface display data that is combined with the data from the standard display buffer on a pixel-by-pixel basis according to data from a mask plane buffer. The interface processor manages input from the tablet, presents feedback to the user by means of the ink and mask planes, and provides keystroke and mouse data to the main processor as if from a standard keyboard controller. The interface processor presents the user with a collection of simulated devices, including standard devices such as a keyboard and a mouse. A nonstandard simulated device performs character recognition, permitting handwritten characters to be used for program input. During interaction with one of the user's programs, the user can activate and deactivate simulated devices (by removing them from and returning them to a device tray) and can make adjustments in their operation and location on the screen.

French Abstract
Systeme informatique comprenant un numeriseur recouvrant l'ecran de visualisation. Plusieurs fonctions du systeme permettent a l'utilisateur d'executer des programmes standard et de dialoguer avec ces derniers qui sont concus pour etre introduits par l'intermediaire d'un clavier ou d'une souris et qui ne sont pas destines a etre utilises avec un numeriseur. En outre, un processeur d'interface vient s'ajouter au processeur principal, dans lequel les programmes de l'utilisateur sont executes. Hormis l'affichage intermediaire standard, il existe un tampon a ecran a encre pour les donnees d'affichage de l'interface qui sont associees aux donnees provenant de l'affichage intermediaire standard sur une base pixel par pixel en fonction des donnees provenant d'un tampon de plan a masque. Le processeur d'interface gere l'entree provenant du numeriseur, presente la retroaction a l'utilisateur a l'aide des plans a masque et a encre, et fournit au processeur principal des donnees de

clavier et de souris de la meme maniere que si elles provenaient d'une commande par clavier standard. Le processeur d'interface presente a l'utilisateur un ensemble de dispositifs simules comprenant des dispositifs standards tels qu'un clavier et une souris. Un dispositif simule special effectue la reconnaissance des caracteres, ce qui permet d'utiliser des caracteres manuscrits pour entrer des programmes. Lorsque l'utilisateur dialogue avec un de ses programmes, il peut lancer ou arreter des dispositifs simules en les sortant d'un chariot de dispositifs ou bien en les renvoyant vers ce dernier et il peut egalement effectuer des modifications au niveau de leur fonctionnement et de leur emplacement sur l'ecran.

Main International Patent Class: **G06F-015/02**
International Patent Class: **G06F-03:033**
Fulltext Availability:
Claims

Claim
... article titled "Digitizer Technology: Performance Characteristics and the
Effects on the User Interface" (IEEE Computer **Graphics** and **Applications** ,
April 1987, pp 31-44) describes digitizer technology. A tablet interface 36 transfers X-Y...connection of a physical keyboard, the optiniizer provides a data register 130 (bidirectional) and status **register** 132 that is **accessed** by the interface processor. The interface processor sends keystrokes (both from the optional physical keyboard...

10/5,K/45 (Item 40 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00182552
SPLIT SCREEN KEYBOARD EMULATOR
EMULATEUR DE CLAVIER A ECRAN DIVISE
Patent Applicant/Assignee:
GRID SYSTEMS CORPORATION,
Inventor(s):
HAWKINS Jeffrey C,
SANFORD Lindsay,
MCNAMARA James H,
DULANEY Kenneth L,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9016032 A1 19901227
Application: WO 90US2953 19900524 (PCT/WO US9002953)
Priority Application: US 89952 19890612
Designated States: AT AU BE CH DE DK ES FI FR GB IT JP KR LU NL SE SU
Main International Patent Class: **G06F-015/20**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 4397

English Abstract
A system for providing keystroke data to an application program without utilizing a keyboard that simultaneously displays application program graphics and a keyboard representation on different segments of a screen (12). Keys are selected by touching the screen (12t) at the location of the graphic representation of the key on the screen (12b). The system is transparent to the application program.

French Abstract
Un systeme sert a fournir des donnees de frappe a un programme d'application sans utiliser un clavier qui affiche simultanement la graphique du programme d'application et une representation de clavier sur

des segments differents d'un ecran (12). Des touches sont choisies en touchant l'ecran (12t) a l'endroit sur l'ecran (12b) ou se trouve la representation graphique de la touche. Le systeme est transparent au programme d'application.

Main International Patent Class: **G06F-015/20**
Fulltext Availability:
Claims
Claim
... invention of claim I wherein said means for providing input keystroke 'data comprises:
a keyboard **scan register** that generates a hardware interrupt signal,when loaded with keystroke data so that the application...

...keyboard,
S. In a computer of the type that includes a screen for displaying the **graphics** of an **application** program being run on the computer, with the application program of the type that processes...data as input data to the application program when the standard software is utilized to **access** the keystroke data storage **register** .
B. In a computer of the type that includes a screen for displaying the **graphics** of an **application** program being run on the computer, with the application program of the type that processes...

10/5,K/46 (Item 41 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00161416
CIRCUITRY SYSTEM FOR ENABLING UPDATE OF ROM DATA WORDS
SYSTEME DE CIRCUIT PERMETTANT DE METTRE A JOUR DES MOTS CONTENANT DES DONNEES ENREGISTREES EN MEMOIRE MORTE (ROM)
Patent Applicant/Assignee:
UNISYS CORPORATION,
Inventor(s):
KUMBASAR Cevat,
Patent and Priority Information (Country, Number, Date):
Patent: WO 8907794 A1 19890824
Application: WO 89US695 19890217 (PCT/WO US8900695)
Priority Application: US 88775 19880219
Designated States: AT BE CH DE FR GB IT JP KR LU NL SE
Main International Patent Class: **G06F-009/26**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 6208

English Abstract
A non-reprogrammable ROM holding microinstruction words cooperates with a Content Addressable Memory made of a TAG Memory and Data Memory. Portions of the locations in the TAG Memory have the same address as certain locations in the ROM so that when these selected addresses occur, a multiplexer will select the updated data from the Data Memory rather that from the ROM. The entire system is placed on one chip and provides great spatial surface savings over that which would be required if only a Static RAM were used for a control storage unit to hold the microinstruction words.

French Abstract
Une memoire morte (ROM) non reprogrammable contenant des mots de microinstructions, coopere avec une memoire associative faite d'une memoire TAG (d'affectation d'adresse symbolique) et d'une memoire de donnees. Des parties des emplacements situes dans la memoire TAG ont les

memes adresses que certains emplacements se trouvant dans une memoire morte, de sorte que lorsque ces adresses selectionnees apparaissent, un multiplexeur selectionne les donnees mises a jour provenant de la memoire de donnees plutot que celles provenant de la memoire morte. Le systeme dans son integralite est place sur une puce et permet d'economiser une place considerable par rapport a celle qui serait necessaire si l'on n'utilisait qu'une memoire vive (RAM) statique pour une unite de stockage de commande afin de conserver les mots de micro-instructions.

Main International Patent Class: **G06F-009/26**
Fulltext Availability:
Claims

Claim
... connected to provide addresses to
said ROM means and to said Content Addressable
Memory means (**CAM**);
(d) means for selecting the accessed data word
output from either said ROM or said CAN.
2o, The combination of claim 1 wherein said **CAM** means
includeso
(a) a TAG Memory having m/r locations where `r"
is equal to...

...includes a multiplexer unit which receives an output from said
R014 means and from said **CAM** means said multiplexer unit
operating to select a data word output according-to the signal...for
temporarily holding
the output word accessed from said ROM means;
(b) a data output **register** for temporarily
holding the data **accessed** from said data
memory; and
(c) wherein said ROM register and said data
register provide...

...data words, each word haming a length
of n bits;
(b) a Content Addressable Memory (**CAM**) means tor
holding updated data words,, each word being
of n bits in order to...

...said
ROM means;
(c) address bus means for simultaneousiy
addressing said ROM means and said **CAM** means;
(d) selection means for providing an output
selection signal to a multiplexer unit when...

...irst Read only Memory (ROM) means for
storing microinstruction words;
(b) a Content Addressable Memory (**CAM**) means including
a RAM TAG Memory means and a
RAM Cata memory means wherein said...

10/5,K/47 (Item 42 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00155763
MULTI-PORT VECTOR REGISTER FILE
FICHIER A REGISTRE VECTORIEL MULTIPORT
Patent Applicant/Assignee:
DIGITAL EQUIPMENT CORPORATION,
Inventor(s):
FOSSUM Tryggve,
MANLEY Dwight P,
McKEEN Francis X,

TEHRANIAN Michael M

Patent and Priority Information (Country, Number, Date):
Patent: WO 8902130 A1 19890309
Application: WO 88US2810 19880816 (PCT/WO US8802810)
Priority Application: US 87499 19870831
Designated States: AT BE CH DE FR GB IT JP LU NL SE
Main International Patent Class: **G06F-015/347**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 13358

English Abstract
A vector register file (35) includes a plurality of read ports (51-55) and write ports (41-43). A control logic (60) is coupled to the vector register file (35) for simultaneously writing through at least two write ports and simultaneously reading from at least two read ports. In addition, a barber pole technique for storing words from a logical vector register circuit accessed as a first number of register subarrays (99) into a second number of memory banks (500-515) is provided to minimize the vector register access conflicts.

French Abstract
Un fichier a registre vectoriel (35) comprend une pluralite de ports de lecture (51-55) et d'ecriture (41-43). Une logique de commande (60) est couplee au fichier a registre vectoriel (35) de maniere a permettre une ecriture simultanee par l'intermediaire d'au moins deux ports d'ecriture et une lecture simultanee a partir d'au moins deux ports de lecture. On utilise en outre une technique de stockage selon une structure helicoidale de mots provenant d'un circuit logique a registre vectoriel, auquel on a acces sous la forme d'un premier nombre de sous-reseaux de registre (99), dans un deuxieme nombre de blocs de memoire (500-515), cette technique permettant de limiter au maximum les conflits d'acces au registre vectoriel.

Main International Patent Class: **G06F-015/347**
Fulltext Availability:
Claims

Claim
... a different slice of register array 99.
In accordance with the present invention, the vector **register** file includes **reading** means, coupled to the **register** array and responsive to **read** selection signals, for simulta neously outputting the stored data from the register array through at...output. The three bit SEL input identifies the element address for one of the five **read** ports.
The vector **register** file of the present invention also includes-first selection means, coupled to the reading means...

...data for each of the multiplexers.
Further in accordance with the present invention, the vector **register** file includes **writing** means, coupled to the **register** array and responsive to **write** selection signals, for si multaneously storing the data into the register -array through at least...Register select logic 250 also receives control sig nals from write logic 220 and routes **write** enable signals to the vector **registers** 100-115, The sixteen **write** enable signals are generated by write logic 220 by decoding the WPORTx VREG SEL signals...address for the port is valid and a read operation will take place. The data **read** from vector **register** 99 is valid about 8 ns after the start of the cycle.
Internally,. the first...

...VREG SEL and the WPORTx VELM ADR signals, Similarly

11/5,K/9 (Item 4 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00905248 **Image available**

COMPUTER BASED VERIFICATION SYSTEM FOR TELECOMMUNICATION DEVICES AND METHOD OF OPERATING THE SAME

SYSTEME DE VERIFICATION GERE PAR ORDINATEUR POUR DES DISPOSITIFS DE TELECOMMUNICATION ET PROCEDE RELATIF AU FONCTIONNEMENT DE CE SYSTEME

Patent Applicant/Assignee:
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Patent Applicant/Inventor:
VANDEWEERD Ivo, Vuurkruisenlaan 1, B-3500 Hasselt, BE, BE (Residence), BE (Nationality), (Designated only for: US)
COENEN Steven, Grootloonstraat 101, B-3840 Borgloon, BE, BE (Residence), BE (Nationality), (Designated only for: US)
Legal Representative:
BIRD William E (et al) (agent), Bird Goen & Co., Vilvoordsebaan 92, B-3020 Winksele, BE,

Patent and Priority Information (Country, Number, Date):
Patent: WO 200239325 A2-A3 20020516 (WO 0239325)
Application: WO 2001BE193 20011108 (PCT/WO BE0100193)
Priority Application: GB 200027258 20001108
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: H04L-012/26
International Patent Class: H04L-029/06
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 15841

English Abstract
A computer apparatus is described for displaying and manipulating sequences of frames of hierarchically organized framed data. The apparatus comprises means for generating a graphical user interface on a display screen, the graphical user interface having means for displaying a representation of a hierarchy of the framed data. The computer apparatus also has a pointing device for selecting a portion of the representation of the hierarchy to generate a control signal, and means responsive to the control signal to display a portion of the framed data corresponding to the selected portion of the representation of the hierarchy. The graphical user interface may be used in a computer based verification system for the analysis and display of a sequence of frames of framed data, comprising: means for generating a frame generator for receiving the frame sequence, the frame generator comprising means for processing the frame sequence in accordance with a protocol to form a modified frame sequence and for associating with each frame a description data structure for that frame, and means for outputting the modified frame sequence and the frame description data structure.

French Abstract
L'invention concerne un dispositif informatique pour afficher et manipuler des sequences de trames de donnees tramees organisees hierarchiquement. Ce dispositif comprend un moyen pour generer une interface utilisateur graphique sur un ecran d'affichage, cette interface utilisateur graphique possedant un moyen pour afficher une representation d'une hierarchie des donnees tramees. Ce dispositif informatique possede egalement un dispositif de pointage permettant de selectionner une partie

de la representation de la hierarchie pour generer un signal de commande, et un moyen apte a reagir a ce signal de commande pour afficher une partie des donnees tramees correspondant a la partie selectionnee de la representation de la hierarchie. L'interface utilisateur graphique peut etre utilisee dans un systeme de verification gere par ordinateur pour l'analyse et l'affichage d'une sequence de trames de donnees tramees, qui comprend : un moyen permettant de generer un generateur de trame pour recevoir la sequence de trame, ce generateur de trame comprenant un moyen pour traiter la sequence de trame en fonction d'un protocole pour former une sequence de trame modifiee et pour associer avec chaque trame une structure de donnees de description pour cette trame, ainsi qu'un moyen permettant d'emettre en sortie la sequence de trame modifiee et la structure de donnees de description de trame.

Legal Status (Type, Date, Text)
Publication 20020516 A2 Without international search report and to be republished upon receipt of that report.
Examination 20021017 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20030103 Late publication of international search report
Republication 20030103 A3 With international search report.

Fulltext Availability:
Claims

Claim
... be determined and examined, e.g. by displaying the traffic data frames using a user **graphics interface** preferably in accordance with the present invention (described later).
Provided the computer system can deal...the user can write any code desired. User customization can include creation of a customized **graphical interface** , reading in and parsing a command file for stimulating some control signals, integration of third...

...The present invention includes a method for hardware/software cosimulation, i.e. the ability to **access** control and status **registers** from a computer program. This computer program can generate a test bench to test the...

...or can contain the code that will ran on an embedded processor. This way of **accessing registers** in the DUT can also be used. The present invention includes reactive test plans. For...

11/5,K/16 (Item 11 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00774598 **Image available**
DEVICE CUSTOMIZED HOME NETWORK TOP-LEVEL INFORMATION ARCHITECTURE
ARCHITECTURE D'INFORMATION DE NIVEAU SUPERIEUR POUR RESEAU DOMOTIQUE PERSONNALISEE EN FONCTION DE DISPOSITIFS
Patent Applicant/Assignee:
SAMSUNG ELECTRONICS CO LTD, 416, Maetan-dong, Paldal-ku, Suwon-city, Kyungki-do 442-373, KR, KR (Residence), KR (Nationality)
Inventor(s):
WANG Dongyan, 440 Oak Grove Drive #302, Santa Clara, CA 95054, US
HUMPLEMAN Richard, 343 Lower Vintners Circle, Fremont, CA 94539, US
Legal Representative:
LEE Young-Pil, The Cheonghwa Bldg, 1571-18 Seocho-dong, Seocho-gu, Seoul 137-073, KR
Patent and Priority Information (Country, Number, Date):
Patent: WO 200108150 A1 20010201 (WO 0108150)
Application: WO 2000KR820 20000727 (PCT/WO KR0000820)
Priority Application: US 99146101 19990727; US 99149515 19990817; US 2000592598 20000612
Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR

LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ
TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: G11B-020/04
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 16614

English Abstract
A method and system for generating a user interface in a plurality of multiple devices connected to the network system for controlling devices that are currently connected to a network. A network system includes a physical layer, wherein the physical layer provides a communication medium that can be used by devices to communicate with each other, and multiple devices connected to the physical layer, one or more of the multiple devices storing information including device information. A plurality of the multiple devices each including an agent adapted for: (a) obtaining information from devices currently connected to the network, the information including device information; (b) generating a user interface description in each of the one or more devices based at least on the obtained information, the user interface description in each device including at least one reference associated with the device information of each of the devices currently connected to the network; and (c) displaying one or more user interfaces each based on one of the one or more user interface descriptions, on one or more devices connected to the network capable of displaying a user interface, for user control of the devices that are currently connected to the network.

French Abstract
Cette invention concerne un procede et un systeme permettant de creer une interface utilisateur au niveau d'une pluralite de dispositifs multiples connectes au systeme reseau pour la commande de dispositifs actuellement relies a un reseau. Un systeme reseau comprend une couche physique, laquelle constitue un moyen de communication reciproque entre dispositifs, et des dispositifs multiples relies a la couche physique, l'un ou plusieurs d'entre eux servant a stocker des informations, dont des informations sur les dispositifs. Plusieurs de ces dispositifs multiples contiennent un agent servant a: (a) obtenir des informations de dispositifs actuellement connectes au reseau, dont des informations sur les dispositifs; (b) generer une description d'interface utilisateur dans le ou les dispositifs en fonction de l'information obtenue, cette description d'interface comprenant a chaque fois au moins une reference en rapport a l'information interface pour chacun des dispositifs actuellement connectes au reseau; et (c) afficher une ou plusieurs interfaces utilisateur basees sur les diverses descriptions d interface et sur un ou plusieurs dispositifs connectes au reseau capables d'afficher une interface utilisateur pour la commande par l'utilisateur des dispositifs actuellement connectes au reseau.

Legal Status (Type, Date, Text)
Publication 20010201 A1 With international search report.
Publication 20010201 A1 Before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments.

Fulltext Availability:
Claims

Claim
... e.g. DTV to change to e.g.,
DTV-BED2 through one of the device **GUI** pages 220. As such, the page 220 is displayed as the **Browser** is launched after a reset. The user

sees
and clicks DVCR ICON graphic, whereby DVCR top level control **GUI** 202 is fetched (with 'Play' button etc.). User clicks one of the buttons e.g. "Configure Device NAME" which is another **GUI** (of hierarchy of control pages for DVCR) with a large selection of different names.
User...

...NAIVIE.HTM file that contained DVCR is changed to some other name). Appearance of the **GUI** 220 is more stable in the event of 'bad citizen' devices having too much or...

...and prevent the bad items from
adversely affecting the appearance of the entire top-level **GUI** 220.
<Device Discovery Architecture>
Referring to FIGS. 9A-C, 1 0, 1 1 example functional...

...Agent 408; and (5) GU I Generation and run-time environment 410 (e.g., Web **Browser** 200 in FIG. 2). Further, FIG. 10 shows an example flow diagram for the DDA...other devices, whereby another device can look up in the
ROM the address of the **Register** and then **write** to that **Register** .
Referring Figure 9B, one or more devices include an IP address configuration agent (FWHCP) 406...

...the HN-Directory page. In each
client device, when Ul description generation is complete, the **GUI** generation and run-time environment 410 (e.g., Web **Browser** 200 in FIG. 2) uses the Ul ...Logo.HTM
are contained in pages 204, and 204) to generate the full top-level **GUI** 220 for display in that client device. Web **Browser** uses HTML file 250 to render
the actual **GUI** graphics, in the process accessing files from the devices
e.g. Icon.HTM, Name.HTM...GUL Further,
manufacturers of devices connected to the network 1 00 can provide their own **GUI** design 202, 204 in each device as desired. In addition later, improved **Browser** and Web technology designs need not be hampered by existing technology.
Non-Ul devices, particularly...

...gateway
function, can also include a Ul Description Generation agent 408 to generate top-level **GUi** descriptions 250, without including **GUI** Generation
and Run-Time processes 410 (e.g., Web **Browser** 200) to generate and display **GUIs** 220. With appropriate address use (e.g., using the RFC1918 private addresses on the local...

...Device Discovery
Agent 404 described above, (2) Ul Description Generation Agent (UIDGA) 408, and (3) **GUI** Generation and Run-Time (e.g., Web **Browser** 200) process 41 0. Referring to FIG. 1 1, in one embodiment, a UIDGA agent...

14/5,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01577824
Method and apparatus for register renaming
Verfahren und Vorrichtung zur Anderung der Namen von Registern
Procede et dispositif pour changer la designation de registres
PATENT ASSIGNEE:
FUJITSU LIMITED, (211467), 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8858, (JP), (Applicant designated States: all)
INVENTOR:
Shebanow, Michael C., 1920 Glenwick Drive, Plano, Texas 75075, (US)
Shen, Gene W., 181A Central Avenue, Mountain View, CA 94043, (US)
Swami, Ravi, 3945 Hamilton Park Drive, San Jose, CA 95130, (US)
Patkar, Niteen A., 160 Carlisle Way, Sunnyvale, CA 94087, (US)
LEGAL REPRESENTATIVE:
Liesegang, Eva (81041), Forrester & Boehmert, Pettenkoferstrasse 20-22, 80336 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 1308837 A2 030507 (Basic)
APPLICATION (CC, No, Date): EP 2003002467 960301;
PRIORITY (CC, No, Date): US 397893 950303
DESIGNATED STATES: AT; BE; CH; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
RELATED PARENT NUMBER(S) - PN (AN):
EP 730225 (EP 96103209)
INTERNATIONAL PATENT CLASS: G06F-009/38; G06F-009/30

ABSTRACT EP 1308837 A2
In a microprocessor, an apparatus is included for coordinating the use of physical registers in the microprocessor. Upon receiving an instruction, the coordination apparatus extracts source and destination logical registers from the instruction. For the destination logical register, the apparatus assigns a physical address to correspond to the logical register. In so doing, the apparatus stores the former relationship between the logical register and another physical register. Storing this former relationship allows the apparatus to backstep to a particular instruction when an execution exception is encountered. Also, the apparatus checks the instruction to determine whether it is a speculative branch instruction. If so, then the apparatus creates a checkpoint by storing selected state information. This checkpoint provides a reference point to which the processor may later backup if it is determined that a speculated branch was incorrectly predicted. Overall, the apparatus coordinates the use of physical registers in the processor in such a way that: (1) logical/physical register relationships are easily changeable; and (2) backup and backstep procedures are accommodated.
ABSTRACT WORD COUNT: 171
NOTE:
Figure number on first page: 2

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 030507 A2 Published application without search report
Examination: 030507 A2 Date of request for examination: 20030205
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200319	1232
SPEC A	(English)	200319	7044
Total word count - document A			8276
Total word count - document B			0
Total word count - documents A + B			8276

...SPECIFICATION physical register identifiers PR0))-PRn)) are stored in ROM 40, they cannot be altered by **writing** operations; hence, the physical **register** identifiers PR0))-PRn)) remain constant for the life of the processor 10.

The CAM 42...the next available free physical register, which in the example is PR6)).

After a physical **register** identifier is **retrieved** from the freelist unit 34, control unit 36 applies 114 the logical register value LR3)) to the **CAM** 42. In effect, this operation **checks** for the current physical **register** assignment for logical register LR3)). In the present example, LR3)) is currently assigned to physical...

...as shown in the register file unit 30. Thus, when LR3)) is applied to the **CAM** 42, a hit will be found which will cause the physical **register** identifier PR3)) to be **read** out of the ROM 40. This physical register identifier PR3)), along with the logical register...

...corresponding to PR5)) is the current assignment. The AV bit corresponding to the old physical **register** (PR3))) is not set. This **manipulation** of the AV bit forestalls any confusion that might arise due to multiple instances of...unit 36 of the register management unit 16. Suppose further again: (1) that the logical **register** value LR3)) is **written** into the **CAM** entry corresponding to the physical identifier entry PR5)) as shown in Figure 3b, thereby assigning...

...in the entry indexed by the instruction sequence #0. The writing of these values into **CAM** 42 and reclaim RAM 50 were described previously with reference to steps 108-122 of...

...to note here are: (1) that there are two instances of LR3)) stored in the **CAM** 42, one corresponding to the currently assigned physical register identifier PR5)), and one corresponding to...

...and its corresponding former physical register identifier PR3)). Thereafter, control unit 36 applies the logical **register** value LR3)) **retrieved** from the reclaim RAM 50 to the **CAM** 42 to determine 166 which physical register is currently assigned to the logical register LR3...

...the present example, the AV bit corresponding to PR5)) is cleared. Thereafter, control unit 36 **writes** 170 the logical **register** value LR3)) into the **CAM** 42 at an entry corresponding to the former physical address identifier. Hence, in the present example, LR3)) is written into the **CAM** entry corresponding to the physical register identifier PR3)). Once that is done, control unit 36...

...CLAIMS particular association of logical registers to physical registers for the checkpoint, the backup procedure comprising:
retrieving the **register** file unit validity bits for the checkpoint;
retrieving the information corresponding to the status of...particular association of logical registers to physical registers for the checkpoint, the backup procedure comprising:
retrieving the **register** file unit validity bits for the checkpoint from the checkpoint memory;
retrieving the information corresponding...

14/5,K/13 (Item 13 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00778871
Method and apparatus for coordinating the use of physical registers in a microprocessor
Verfahren und Vorrichtung zum Koordinieren der Benutzung von physikalischen Registern in einem Mikroprozessor
Methode et appareil pour coordonner l'utilisation de registres physiques dans un microprocesseur
PATENT ASSIGNEE:
FUJITSU LIMITED, (211467), 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8858, (JP), (Proprietor designated states: all)
INVENTOR:

Tovey, DeForest W., 14165 Old Japanese Road, Los Gatos, CA 95030, (US)
Shebanow, Michael C., 1920 Glenwood Drive, Plano, TX 75075, (US)
Gmuender, John, 107 Killam Court, Suite B2, Cary, North Carolina 27513, (US)
LEGAL REPRESENTATIVE:
Liesegang, Roland, Dr.-Ing. (7741), FORRESTER & BOEHMERT
Pettenkoferstrasse 20-22, 80336 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 727735 A2 960821 (Basic)
EP 727735 A3 970702
EP 727735 B1 020828
APPLICATION (CC, No, Date): EP 96101841 960208;
PRIORITY (CC, No, Date): US 388364 950214
DESIGNATED STATES: AT; BE; CH; DE; DK; ES; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
INTERNATIONAL PATENT CLASS: G06F-009/34; G06F-012/10
CITED PATENTS (EP B): EP 297265 A; EP 301220 A; EP 514763 A; EP 515166 A; EP 606697 A
CITED REFERENCES (EP B):
PROCEEDINGS OF THE ANNUAL INTERNATIONAL SYMPOSIUM ON MICROARCHITECT, AUSTIN, DEC. 1 - 3, 1993, no. SYMP. 26, 1 December 1993, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 202-213, XP000447502 MOUDGILL M ET AL: "REGISTER RENAMING AND DYNAMIC SPECULATION: AN ALTERNATIVE APPROACH";

ABSTRACT EP 727735 A2

In a microprocessor, an apparatus is included for coordinating the use of physical registers in the microprocessor. Upon receiving an instruction, the coordination apparatus extracts source and destination logical registers from the instruction. For the destination logical register, the apparatus assigns a physical address to correspond to the logical register. In so doing, the apparatus stores the former relationship between the logical register and another physical register. Storing this former relationship allows the apparatus to backstep to a particular instruction when an execution exception is encountered. Also, the apparatus checks the instruction to determine whether it is a speculative branch instruction. If so, then the apparatus creates a checkpoint by storing selected state information. This checkpoint provides a reference point to which the processor may later backup if it is determined that a speculated branch was incorrectly predicted. Overall, the apparatus coordinates the use of physical registers in the processor in such a way that: (1) logical/physical register relationships are easily changeable; and (2) backup and backstep procedures are accommodated. (see image in original document)
ABSTRACT WORD COUNT: 196
NOTE:
Figure number on first page: 1

LEGAL STATUS (Type, Pub Date, Kind, Text):

Assignee:	011017	A2	Transfer of rights to new applicant: FUJITSU LIMITED (211467) 1-1, Kamikodanaka 4-chome, Nakahara-ku Kawasaki-shi, Kanagawa 211-8858 JP
Application:	960821	A2	Published application (A1with Search Report ;A2without Search Report)
Lapse:	030528	B1	Date of lapse of European Patent in a contracting state (Country, date): GR 20020828, NL 20020828, PT 20021210,
Grant:	020828	B1	Granted patent
Lapse:	030514	B1	Date of lapse of European Patent in a contracting state (Country, date): GR 20020828,
Search Report:	970702	A3	Separate publication of the European or International search report
Examination:	980211	A2	Date of filing of request for examination: 971212
Examination:	990421	A2	Date of despatch of first examination report: 990304

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	71
CLAIMS B	(English)	200235	1606
CLAIMS B	(German)	200235	1503
CLAIMS B	(French)	200235	1791
SPEC A	(English)	EPAB96	6712
SPEC B	(English)	200235	6680
Total word count - document A			6784
Total word count - document B			11580
Total word count - documents A + B			18364

...SPECIFICATION sub(0))-PR(sub(n)) are stored in ROM 40, they cannot be altered by **writing** operations; hence, the physical **register** tags PR(sub(0))-PR(sub(n)) remain constant for the life of the processor... available free physical register, which in the example is PR(sub(6)).

After a physical **register** tag is **retrieved** from the freelist unit 34, control unit 36 applies 114 the logical register value LR(sub(3)) to the **CAM** 42. In effect, this operation **checks** for the current physical **register** assignment for logical register LR(sub(3)). In the present example, LR(sub(3)) is...

...in the register file unit 30. Thus, when LR(sub(3)) is applied to the **CAM** 42, a hit will be found which will cause the physical register tag PR(sub...unit 36 of the register management unit 16. Suppose further again: (1) that the logical **register** value LR(sub(3)) is **written** into the **CAM** entry corresponding to the physical tag entry PR(sub(5)) as shown in Fig. 3b...

...in the entry indexed by the instruction sequence #0. The writing of these values into **CAM** 42 and reclaim RAM 50 were described previously with reference to steps 108-122 of...

...here are: (1) that there are two instances of LR(sub(3)) stored in the **CAM** 42, one corresponding to the currently assigned physical register tag PR(sub(5)), and one...

...corresponding former physical register tag PR(sub(3)). Thereafter, control unit 36 applies the logical **register** value LR(sub(3)) **retrieved** from the reclaim RAM 50 to the **CAM** 42 to determine 166 which physical register is currently assigned to the logical register LR ...

...example, the AV bit corresponding to PR(sub(5)) is cleared. Thereafter, control unit 36 **writes** 170 the logical **register** value LR(sub(3)) into the **CAM** 42 at an entry corresponding to the former physical address tag. Hence, in the present example, LR(sub(3)) is written into the **CAM** entry corresponding to the physical register tag PR(sub(3)). Once that is done, control...

...SPECIFICATION physical register tags PR0))-PRn)) are stored in ROM 40, they cannot be altered by **writing** operations; hence, the physical **register** tags PR0))-PRn)) remain constant for the life of the processor 10.

The CAM 42...the next available free physical register, which in the example is PR6)).

After a physical **register** tag is **retrieved** from the freelist unit 34, control unit 36 applies 114 the logical register value LR3)) to the **CAM** 42. In effect, this operation **checks** for the current physical **register** assignment for logical register LR3)). In the present example, LR3)) is currently assigned to physical...

...as shown in the register file unit 30. Thus, when LR3)) is applied to the **CAM** 42, a hit will be found which will cause the physical **register** tag PR3)) to be **read** out of the ROM 40. This physical register tag PR3)), along with the logical register...

...corresponding to PR5)) is the current assignment. The AV bit corresponding to the old physical **register** (PR3))) is not set. This

causing said exception condition;

means for **retrieving** from said **register** reclaim file unit (32) a logical register value and a corresponding physical register tag corresponding to said instruction sequence number;

means for applying said **retrieving** logical **register** value to said content addressable memory (42) to determine a current physical register assigned to...

...clearing a location in said address valid RAM (46) corresponding to the currently assigned physical **register** ;

means for **writing** the logical **register** value **retrieved** from said **register** reclaim file unit (32) into the content addressable memory (42) at an entry corresponding to...

14/5,K/14 (Item 14 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00778870
Method and apparatus for efficiently writing **results to renamed** registers
Verfahren und Vorrichtung zum effizienten Schreiben der Ergebnisse in Registern mit geandertem Namen
Methode et appareil pour ecrire efficacement des resultats dans des registres renommes
PATENT ASSIGNEE:
HAL COMPUTER SYSTEMS, INC., (1500960), 1315 Dell Avenue, Campbell, CA 95008, (US), (applicant designated states: AT;BE;CH;DE;DK;ES;FR;GB;GR;IE;IT;LI;LU;MC;NL;PT;SE)
INVENTOR:
Tovey, DeForest W., 14165 Old Japanese Road, Los Gatos, CA 95030, (US)
Shebanow, Michael C., 1920 Glenwood Drive, Plano, TX 75075, (US)
Gmuender, John, 107 Killam Court, Suite 2B, Cary, North Carolina, 27513, (US)
LEGAL REPRESENTATIVE:
Liesegang, Roland, Dr.-Ing. (7741), FORRESTER & BOEHMERT Franz-Joseph-Strasse 38, 80801 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 727736 A2 960821 (Basic)
EP 727736 A3 970416
APPLICATION (CC, No, Date): EP 96101840 960208;
PRIORITY (CC, No, Date): US 388606 950214
DESIGNATED STATES: AT; BE; CH; DE; DK; ES; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
INTERNATIONAL PATENT CLASS: G06F-009/345; G06F-009/38;

ABSTRACT EP 727736 A2
A method and apparatus stores result data from an execution unit into a physical destination register in a register renaming superscaler microprocessor. The destination register number is associated with the result data and sent to a decoder which decodes the destination register number and enables the destination register corresponding to the destination register number to accept the result data broadcast to the physical destination registers. (see image in original document)
ABSTRACT WORD COUNT: 83

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 960821 A2 Published application (A1with Search Report ;A2without Search Report)
Search Report: 970416 A3 Separate publication of the European or International search report
Examination: 971126 A2 Date of filing of request for examination: 970924
Examination: 980422 A2 Date of despatch of first examination report: 980305

Withdrawal: 990310 A2 Date on which the European patent application was deemed to be withdrawn: 980916
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	371
SPEC A	(English)	EPAB96	1083
Total word count - document A			1454
Total word count - document B			0
Total word count - documents A + B			1454

Method and apparatus for efficiently writing **results to renamed** registers

...SPECIFICATION in one section of the microprocessor, another portion of the microprocessor assigns the physical destination **register** to that instruction, by **writing** the instruction's tag into a **CAM** . After the instruction executes, the result data and the instruction tag are broadcast to all of the CAMs corresponding to each possible destination register. Each **CAM** listens to the tags broadcast and the **CAM** which contains the matching tag enables the corresponding register to accept the data. Thus, the result data is **written** to the **register** .
Because the tags must be unique, they are often quite large, making the CAMs in...

14/5,K/35 (Item 35 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00432224
Graphics display split-serial register system
Graphisches Anzeigesystem mit einem geteilten seriellen Register
Systeme graphique d'affichage comportant un registre seriel divise
PATENT ASSIGNEE:
TEXAS INSTRUMENTS INCORPORATED, (279070), 13500 North Central Expressway, Dallas Texas 75265, (US), (applicant designated states: DE;FR;GB;IT;NL)
INVENTOR:
Ing-Simmons, Nicholas Kerin, 74 Lincroft, Oakley, Bedford, MK437SS, (GB)
Robertson, Iain Craig, No. 2 Marina Court, Bedford, MK42EE, (GB)
LEGAL REPRESENTATIVE:
Abbott, David John et al (27491), Abel & Imray Northumberland House 303-306 High Holborn, London, WC1V 7LH, (GB)
PATENT (CC, No, Kind, Date): EP 410743 A2 910130 (Basic)
EP 410743 A3 920513
EP 410743 B1 960221
APPLICATION (CC, No, Date): EP 90308184 900726;
PRIORITY (CC, No, Date): US 387569 890728
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: G09G-001/16;
CITED PATENTS (EP A): US 4689741 A; EP 245564 A

ABSTRACT EP 410743 A2
A graphical data presentation circuit and method which allows for tightly packing a video memory (130) without regard for the pixel size or number of pixels on a line of the graphic display. The memory output split-serial register (140) is used together with a counter (94) to maintain count of the currently executing output stage of the register (140). When a first half of the register (140) has completed transferring its data to the display it is cleared and reloaded with the first part of the next memory row. When the second half of the register (140) is likewise finished transferring its data it is also cleared and reloaded with the data from the second half of the memory row. This alternating operation allows for mid-row register refreshing without affecting data transfer performance. (see image in original document)
ABSTRACT WORD COUNT: 142

LEGAL STATUS (Type, Pub Date, Kind, Text):

Lapse:	030212	B1	Date of lapse of European Patent in a contracting state (Country, date): NL 19960221,
Application:	910130	A2	Published application (Alwith Search Report ;A2without Search Report)
Search Report:	920513	A3	Separate publication of the European or International search report
Examination:	930107	A2	Date of filing of request for examination: 921102
Examination:	940622	A2	Date of despatch of first examination report: 940505
Grant:	960221	B1	Granted patent
Oppn None:	970219	B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPAB96	795
CLAIMS B	(German)	EPAB96	764
CLAIMS B	(French)	EPAB96	917
SPEC B	(English)	EPAB96	6968
Total word count - document A			0
Total word count - document B			9444
Total word count - documents A + B			9444

...SPECIFICATION selected, clock 2001, operating in conjunction with the memory shift clock, serves to increment the **tap** point shift **register** in conjunction with data being **read** from the serial **register** . Thus, when the **tap** point **register** contains all 111's it signifies that the data from position 111 of half- **register** A, FIGURE 6, is being **read** to the bus. This corresponds to pixel 46, memory bit B7. The tap point counter...

...half-register B where memory positions B8 to B15 are in turn sent to the **graphics display** . Note that the register operation just described does not control the actual shifting out of...

...CLAIMS rows.
4. The graphics processing system according to claim 3, further comprising:
an established shift **register** mask (93); and
a **tap** point shift **register** (91) containing bits representative of said first data position, said tap point bits being created...

...the data storage positions on said split register beginning with the position within said split **register** corresponding to said **tap** point.
11. A method according to claim 10, further including the steps of:
loading a...

14/5,K/36 (Item 36 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00431259
Apparatus and method for reading, writing and refreshing memory with direct virtual or physical access
Verfahren und Anordnung zum Lesen, Schreiben und Auffrischen eines Speichers mit direktem virtuellem oder physikalischem Zugriff
Dispositif et procede de lecture, ecriture et rafraichissement de memoire avec acces physique ou virtuel direct
PATENT ASSIGNEE:
TANDEM COMPUTERS INCORPORATED, (524030), 19333 Vallco Parkway, Cupertino California 95014-2599, (US), (applicant designated states: DE;FR;GB;IT;SE)
INVENTOR:
Horst, Robert W., 2804 Robeson Park Drive, Champaign, Illinois 61821, (US)

Shah, Ajay K., 2729 Mathias Court, San Jose, California 95121, (US)
Yamamoto, I. Ko, 3436 Lochinvar Avenue, Santa Clara, California 95051, (US)
LEGAL REPRESENTATIVE:
Ayers, Martyn Lewis Stanley et al (42851), J.A. KEMP & CO. 14 South Square Gray's Inn, London WC1R 5LX, (GB)
PATENT (CC, No, Kind, Date): EP 407119 A2 910109 (Basic)
EP 407119 A3 920923
EP 407119 B1 970910
APPLICATION (CC, No, Date): EP 90307198 900702;
PRIORITY (CC, No, Date): US 375428 890703
DESIGNATED STATES: DE; FR; GB; IT; SE
INTERNATIONAL PATENT CLASS: G06F-012/10;
CITED PATENTS (EP A): GB 2193017 A; WO 8900730 A; WO 8900730 A; WO 8900730 A; WO 8605917 A; WO 8605917 A; WO 8605917 A; EP 239359 A
CITED REFERENCES (EP A):
PATENT ABSTRACTS OF JAPAN, vol. 9, no. 76 (P-346)(1799), 5th April 1985; & JP-A-59 207 082 (NIPPON DENKI K.K.) 24-11-1984;

ABSTRACT EP 407119 A2

A computer memory system is provided. Received memory requests can be for addresses which are virtual or physical. The type of address is determined, and a virtual/physical bit is set and stored. At least row address bits are compared to one or more registers which contain either a virtual or a physical row address, corresponding to a row addressed by a row address latch. When there is a hit with respect to one of these registers, column address bits are used to select the requested memory element, without the necessity for a virtual-to-physical translation. When there is a miss on all **registers** , a physical address is **obtained** , either from the requested address when this is physical, or from a virtual-to-physical translation. The physical address is used to load a new row address into a row address latch. Some column address bits are changed only when there has been a miss. A refresh cycle is described, which includes reading back into a row address latch the same row address which occupied the row address latch before the refresh cycle, thus preserving locality information or structure. (see image in original document)
ABSTRACT WORD COUNT: 193

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	910109	A2	Published application (A1with Search Report ;A2without Search Report)
Search Report:	920923	A3	Separate publication of the European or International search report
Examination:	930224	A2	Date of filing of request for examination: 921221
Change:	940713	A2	Representative (change)
Examination:	960228	A2	Date of despatch of first examination report: 960112
Grant:	970910	B1	Granted patent
Oppn None:	980902	B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9709W1	816
CLAIMS B	(German)	9709W1	734
CLAIMS B	(French)	9709W1	974
SPEC B	(English)	9709W1	13701
Total word count - document A			0
Total word count - document B			16225
Total word count - documents A + B			16225

...ABSTRACT the necessity for a virtual-to-physical translation. When there is a miss on all **registers** , a physical address is **obtained** , either from the requested address when this is physical, or from a virtual-to-physical...

...SPECIFICATION error correction code check bit generators 70, 72, and

thence to the latches in the **write** data **register**...

In the process depicted in Fig. 4, the MEMOP state machine 114 determines that...

...column address strobe and write enable causes transfer of the write data 446 from the **write** data **register** 52 to one of the memory banks 32, 34, 36, 38. Following the transfer, the...through the first two column/row multiplexers 54, 56 to the address latches of the **write** data **register** 52. At the same time, bits 15 and 16 of the row address are sent...

...60, 62, 64 are switched to "column" 580, and the memory access which caused the **CAM** miss is retried 582.

As noted above, in the preferred embodiment, the computing environment contains...

?